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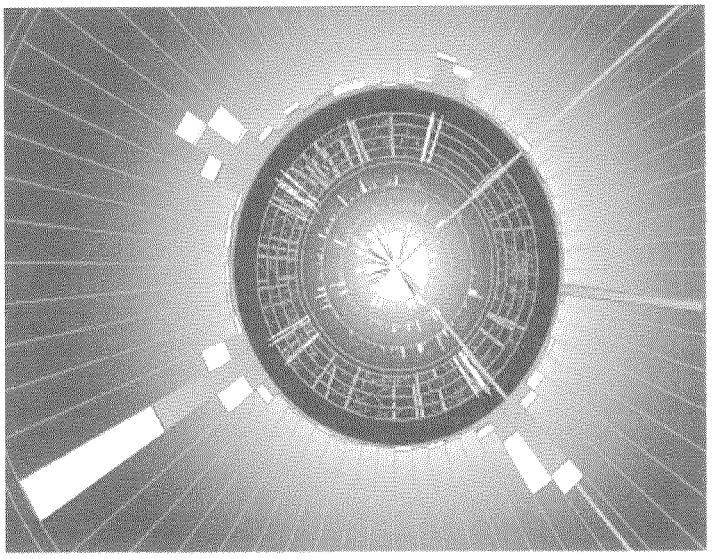
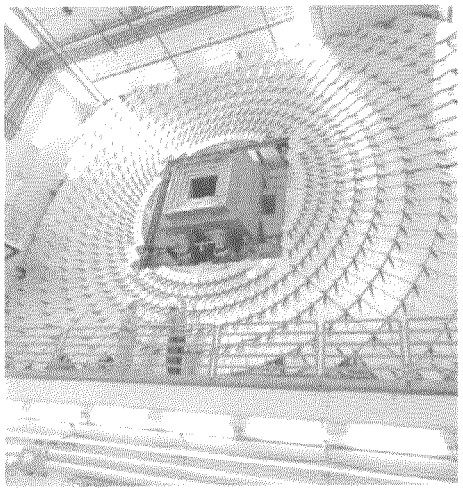
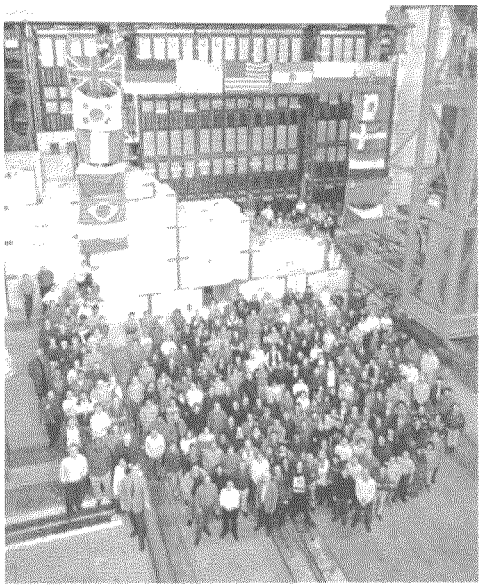
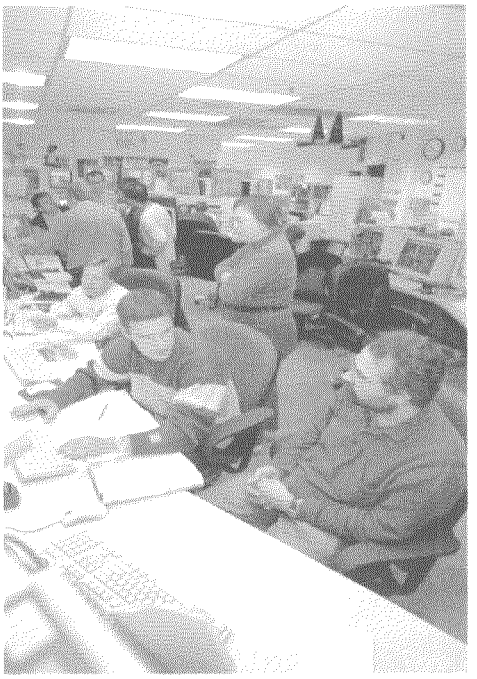
Run IIb Upgrade Technical Design Report









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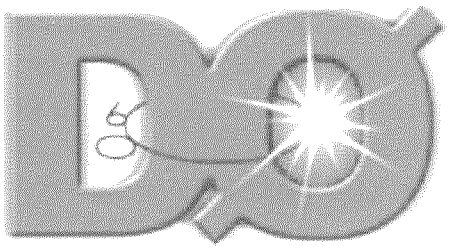
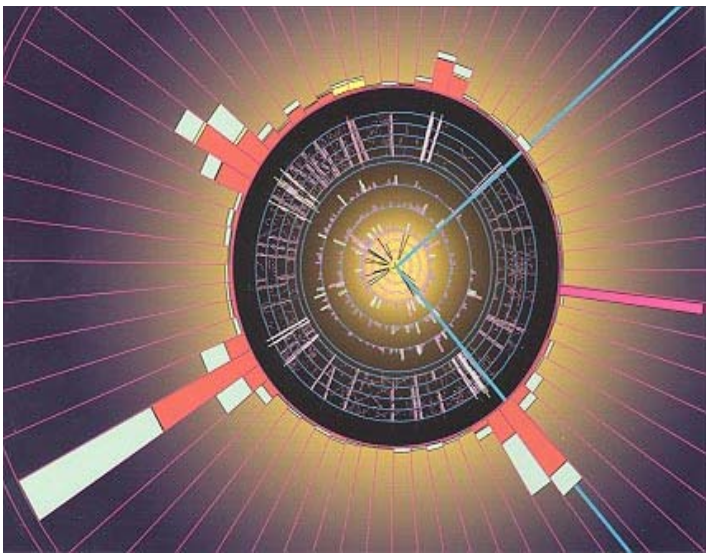


DØ Collaboration

September 12, 2002

Run IIb Upgrade Technical Design Report



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September 12, 2002

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DØ Run IIb Upgrade Technical Design Report

PREFACE

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PREFACE

There is broad agreement within the experimental and theoretical high-energy physics communities that the most pressing issue facing particle physics is the search for the origin of mass. More specifically, we seek to understand the mechanism by which the W and Z particles that mediate the weak force gain mass, while the photon, which has the same couplings to matter, remains massless. In the Standard Model of particle interactions, this electroweak symmetry breaking occurs through interactions with a so-far unobserved particle, called the Higgs boson. Furthermore, within the Standard Model framework, the Higgs particle is responsible for the masses of all the known particles. Searching for the Higgs has become the highest priority in the High Energy Physics community, not only because it is the last undiscovered particle of the Standard Model, but also because its unique role within the Standard Model provides a window that may help us understand the new physics that must be present at higher mass scales.

The Tevatron Collider at Fermilab is currently the only facility in the world capable of making a Higgs discovery. Simulation studies have shown that the two Tevatron Collider experiments, CDF and DØ, are sensitive to the Higgs over almost all of its presently allowed mass range. Our goal is to accumulate sufficient data to make a sensitive search for the Higgs that will have a high probability of success if the Standard Model predictions are correct.

These goals cannot be achieved without upgrades to the DØ detector. The silicon tracking detector is not expected to survive beyond the 2-4 fb^{-1} of integrated luminosity that will be delivered during Run IIa, well short of the 15 fb^{-1} goal for Run IIb. The corresponding increase in instantaneous luminosity necessitates upgrading the trigger system to maintain high trigger efficiency for the Higgs search and other elements of the Run IIb physics program while providing the required background rejection. Finally, data acquisition (DAQ) and online computing upgrades are needed to continue efficient operation of the experiment beyond Run IIa.

This document presents the technical design for the DØ Run IIb upgrades. It is divided into five parts, covering the Run IIb physics goals, the Silicon Detector, the Trigger Upgrade, DAQ/Online Computing, and Installation. Each part is organized so that it is self-contained, providing the motivation, goals, and technical description of the proposed upgrade. A brief summary concludes this report.

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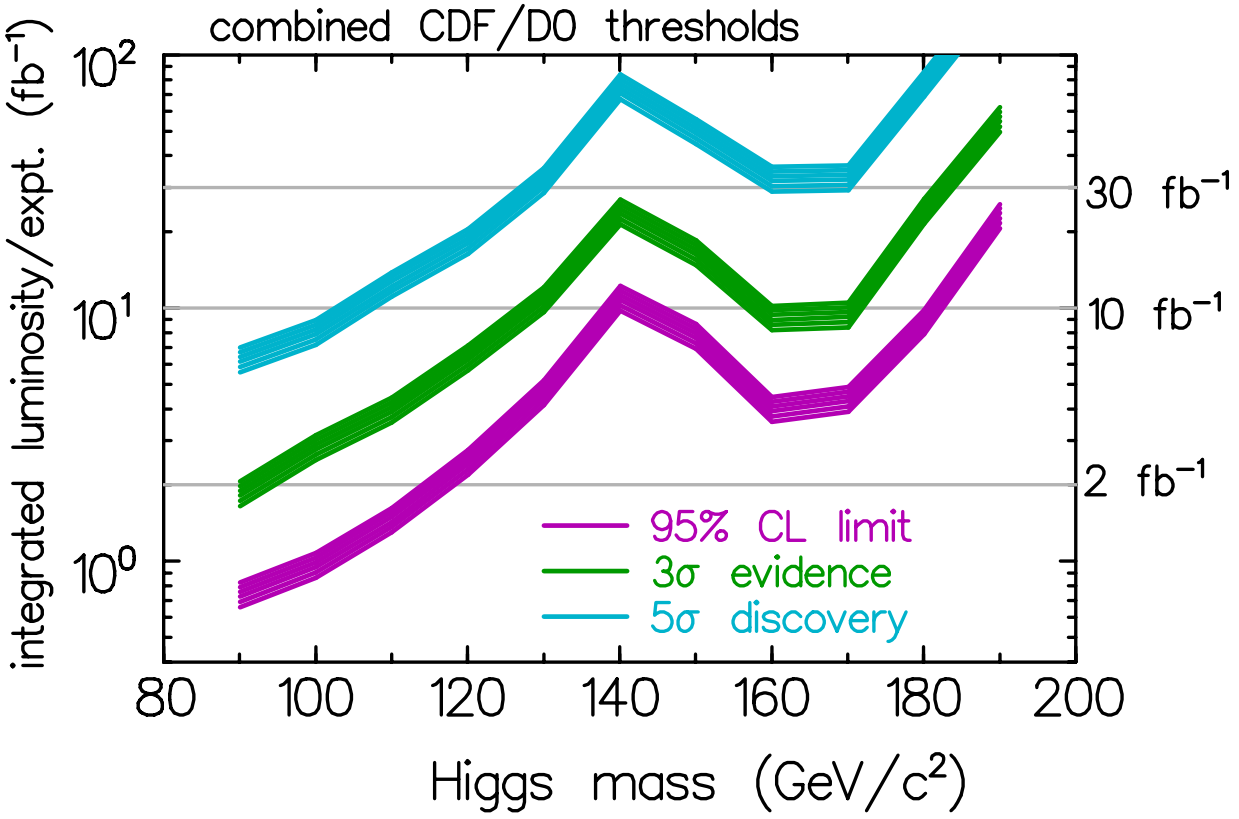
DØ Run IIb Upgrade Technical Design Report



PHYSICS GOALS

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PHYSICS GOALS CONTENTS

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1 INTRODUCTION

Proton-antiproton collisions at $\sqrt{s} = 2$ TeV have proved to be a very fruitful tool for deepening our understanding of the standard model and for searching for physics beyond this framework. DØ has published more than a hundred papers from Run I, including the discovery and precision measurements of the top quark, precise tests of electroweak predictions, QCD tests with jets and photons, and searches for supersymmetry and other postulated new particles. With the addition of a magnetic field, silicon and fiber trackers, and substantial upgrades to other parts of the detector, DØ has started with the goal of building on this broad program, taking advantage of significantly higher luminosities, and adding new measurements in b-physics. The strengths of the DØ detector are its liquid argon calorimetry, which provides outstanding measurements of electrons, photons, jets and missing E_T; its large solid angle, multi-layer muon system and robust muon triggers; and its state of the art tracking system using a silicon detector surrounded by a fiber tracker providing track triggers.

A series of physics workshops organized by Fermilab's Theory group together with the CDF and DØ collaborations has mapped out the physics terrain of the Tevatron in some detail. It is clear from the very large amount of work carried out in these meetings and described in the reports[1] that integrated luminosities much higher than the $2fb^{-1}$, which was the original goal of Run II, add significantly to the program. While all areas of physics benefit from increased statistics, it is the very real possibility of discovering the standard model Higgs boson (or its supersymmetric versions) and/or supersymmetric particles or other physics beyond the standard model, that forms the core motivation for the Laboratory's luminosity goal of 15 fb^{-1} per detector. We have therefore used the most promising Higgs discovery channels as benchmark processes for the Run IIb upgrade, which is described in this design report, and have optimized the detector configuration for them. All other high p_T physics programs benefit from this detector optimization (though for the QCD and b-physics programs the benefits will be balanced by decreased trigger allocations and some loss of geometric acceptance). In the following, we discuss physics requirements on the Run IIb upgrade imposed by Higgs searches and their implications for other high p_T physics programs.

[1] http://fnth37.fnal.gov/run2.html

2 STANDARD MODEL HIGGS BOSON SEARCHES

The highest cross section Higgs production channel at the Tevatron is the gluon fusion reaction $gg \rightarrow H$. Unfortunately, for Higgs masses below about 135 GeV, its dominant decay mode is to $b\bar{b}$ and is swamped by QCD production of b-jets. The most promising Higgs search strategy in this mass range is to focus on associated production of a Higgs with a W or Z boson, $p\bar{p} \rightarrow WH$ and $p\bar{p} \rightarrow ZH$. The leptonic decays of the W and Z enable a much better signal to background ratio to be achieved, but one must pay the cost of a production cross section about one fifth that of inclusive production together with the leptonic branching ratios of the vector bosons. This relatively low signal cross section times branching ratio motivates the need for high integrated luminosity. In turn, the need for high integrated luminosity forces the accelerator to operate in a mode where each high p_T event is likely to be accompanied by a significant number of low p_T "minimum bias" events occurring in the same $p\bar{p}$ bunch crossing. The mean number of interactions <n> is around 5 for a luminosity of $2\times10^{32}cm^{-2}s^{-1}$ at 132ns bunch spacing. This high occupancy environment is one of the main challenges for Run IIb.

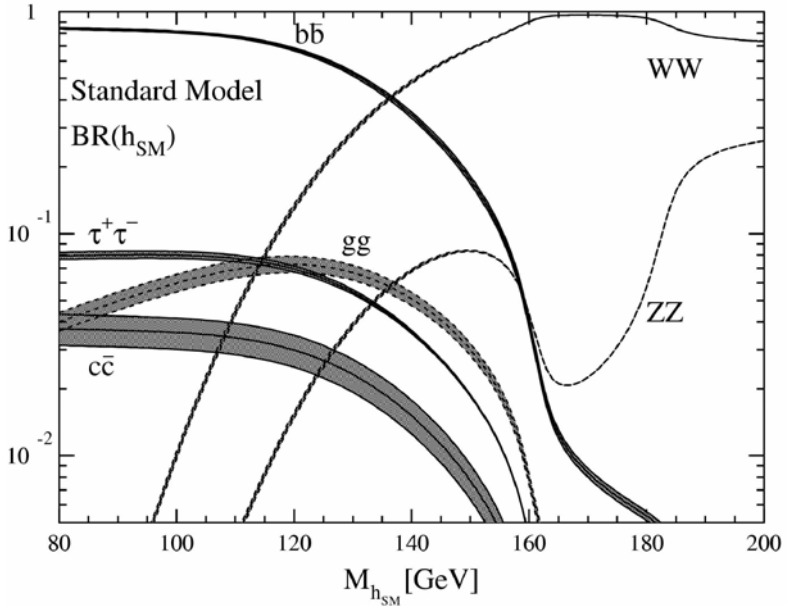

Figure 1 - Standard Model Higgs decay branching ratios as a function of Higgs mass.

Figure 1 shows the decay modes of the Standard Model Higgs in the mass range relevant to DØ. For Higgs masses below roughly 135 GeV, the Higgs decays dominantly to b-quark pairs, and for masses above this (but less than the $t\bar{t}$ threshold) the decay is dominantly to W and Z boson pairs. Thus, searches for Higgs boson in the low mass region $M_H < 135$ GeV must assume $H \rightarrow b\bar{b}$ decays. Searches for the lightest Higgs in supersymmetric models must also assume decay to b-quark pairs.

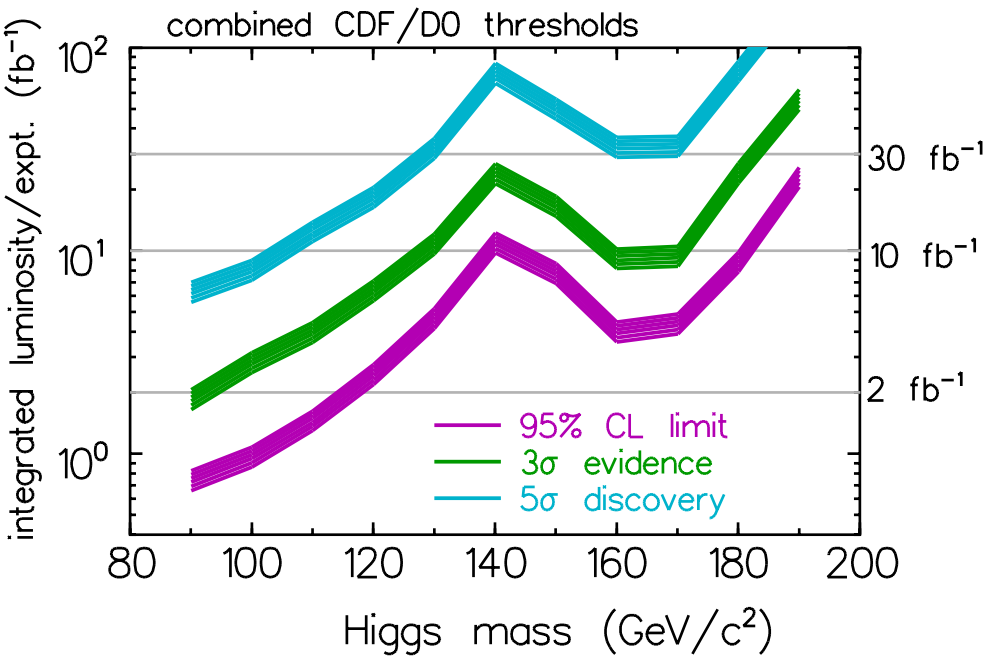

Figure 2 - Required luminosity as a function of Higgs mass for 95% C.L. exclusion, 3σ evidence, and 5σ discovery.

Figure 2 shows the luminosity required to exclude or discover a Standard Model Higgs at the Tevatron. This result assumes the expected Run IIa performance of both the CDF and DØ detectors. For 15 fb^{-1}, a 5σ discovery can be made for a Higgs mass of 115 GeV, a >3σ signal is expected for most of the mass range up to 175 GeV, and Higgs masses up to 180 GeV can be excluded if there is no sign of the Higgs.

As stated above, for Higgs bosons in the low mass range, the associated-production modes will be used for searches. The final states of interest are those where the W(Z) boson decays to charged leptons or neutrinos, and at least two b-flavored hadronic jets from the Higgs decay are selected. The dominant background arises from W(Z) bosons produced in association with jets from initial state radiation of gluons. Even in the associated production channels, the intrinsic signal to background for vector boson plus two jets is prohibitively small. However, the majority of the W(Z)+jets background contains light quark or gluon jets, while the Higgs signal is almost exclusively $b\bar{b}$. The ability to identify the b-jets from Higgs decay is the crucial first step in reducing the boson+jets background to a manageable level. The combination of b-jet identification, reconstructed dijet mass, and additional kinematic variables is used to improve the signal to noise to achieve the sensitivity shown in Figure 2. This result depends on the ability to identify b-jets with at least 50% efficiency and background contamination from light quark jets at the 1% level. Effective tagging of b-jets is one the most important physics objectives for the tracker system. It is likely that two tagged jets will be required to reduce the background to acceptable levels, so maximizing the tagging efficiency is most important.

The identification of b-jets can be done by exploiting either the relatively long lifetime of the b-flavored particles or by detecting leptons from semi-leptonic decay of b-quarks (or both). The first technique allows all decays to be considered, whereas the second method suffers reduced

statistical precision because of the ~30-40% decay branching ratio of b-quarks to final states including leptons. The long lifetime of the b-quarks is reflected in a B-meson decay that occurs some distance from the primary beam interaction point. For b-flavored particles with energies expected from Higgs decay, the mean decay length is 2 mm, and the mean impact parameter is roughly 250 μm. Thus, efficiently and cleanly identifying these decays requires a detector with the ability to reconstruct tracks with an impact parameter resolution in the tens of microns. The most feasible technology for this is silicon microstrip detectors.

One of the low-mass Higgs signatures is particularly noteworthy: Higgs production in association with a Z boson, which decays into a neutrino-antineutrino pair, resulting in missing energy and two b-jets in the final state. One of the main strengths of the DØ detector is its good missing energy identification; yet to keep trigger rates under control the present threshold on the missing E_T trigger is about 35 GeV. A search for the Higgs boson in the ZH channel can certainly benefit from a lower trigger threshold. This can be achieved by implementing an efficient 2-jet trigger at the first trigger level and using information about displaced tracks at the second trigger level. The proposed calorimeter trigger upgrade will enable us to efficiently trigger on jets of moderate transverse energy, while the silicon track trigger upgrade will retain our ability to trigger on displaced tracks with the upgraded silicon tracker.

Searches for the Higgs boson in the intermediate mass region $135<M_H<200$ GeV/c^2 assume inclusively-produced Higgs decaying to WW* and ZZ*, where at least one of the vector bosons decays to leptons. Effective lepton triggering and identification, essential for vector boson detection, is important for Higgs searches in both low and intermediate mass regions. The tracking system plays a crucial role in electron, muon and, arguably, tau lepton triggering and identification. Leptons from W and Z decays are fairly energetic, with $p_T>20$ GeV/c. The requirement that we efficiently trigger on high-p_T tracks is the primary motivation for the track trigger upgrade and the cal-track match system, while the requirement that we efficiently reconstruct these tracks is an important design requirement for the silicon tracker upgrade.

Higgs production in association with $t\bar{t}$ has received a lot of attention recently[2]. Though low in cross section, this channel provides a very rich signature with leptons, missing energy, and 4 b-jets in the final state. B-jets produced in this process have higher energy than those in processes such as WH production. Tracks in such jets tend to be more collimated, emphasizing the need for robust pattern recognition in the high occupancy environment. Another challenge for this channel is ambiguity in b-jet assignment, which can be reduced if the charge of the b-quark can be tagged. Several methods for b-charge tagging have been developed so far, e.g. same side tagging, jet charge tagging. Having information about charge of tracks in the secondary and tertiary b-decay vertices could be invaluable to improve purity of these tagging methods. This puts additional emphasis on precise impact parameter reconstruction.

[2] J. Goldstein *et al*., "$p\bar{p} \to t\bar{t}H$: A discovery mode for Higgs boson at the Tevatron", Phys. Rev. Lett. **86**, 1694 (2001).

It is important to note that Higgs searches at the Tevatron and at the LHC are complementary to each other. While LHC experiments[3] emphasize the $gg \to H \to \gamma\gamma$ channel, where Higgs is produced and decays via loop diagrams, the Tevatron's emphasis is on tree-level production and tree-level decay. For a Standard Model Higgs, the branching ratio to $\gamma\gamma$ is very low, making it impossible to observe this channel at the Tevatron. However, some models predict a "bosophilic" Higgs, for which this decay mode is enhanced. Thus, high-energy photon identification is important for Higgs search beyond the Standard Model. Photon/electron separation is essential for high-purity photon identification. For this purpose the tracking system must ensure low fake track rate and a good momentum resolution.

3 PHYSICS BEYOND THE STANDARD MODEL

Searches for SUSY and strong dynamics will benefit from the requirements imposed on the tracking system by the Standard Model Higgs searches. SUSY extensions of the Standard Model predict two Higgs doublets with five physical Higgs bosons – two neutral scalars (h,H), one neutral pseudoscalar (A) and two charged bosons ($H^{\pm}$). Over much of the remaining allowed parameter space, the lightest neutral boson h behaves similarly to the Standard Model Higgs, and has a mass in the range 115-130 GeV, while the H, A and $H^{\pm}$ masses are larger. The standard model Higgs searches described above are, at the same time, searches for the lightest SUSY Higgs h. In addition, some Higgs cross sections are enhanced in SUSY, e.g. $p\bar{p} \to b\bar{b}(A/h)$ with $A,h \to b\bar{b}$ in a high $\tan\beta$ scenario. Efficient b-jet triggering, tagging, and b-charge identification is essential for Higgs discovery in these channels, which contain four b-jets. The charged Higgs boson can be detected in top decays or through pair production of H^+H^-, and decays to $b\bar{c}$ or $\tau^-\nu$, depending on $\tan\beta$. Again, good heavy flavor triggering, tagging, and tracking (for tau-lepton identification) are important. Studies have shown that the Tevatron can exclude almost the whole plane of SUSY Higgs parameters (m_A, tan β) at the 95% level, if no signal is seen in 5 fb^{-1}, and can discover at least one SUSY Higgs at the 5 standard deviation level with 15-20 fb^{-1} per experiment.

[3] M. Carena, S. Mrenna, C. Wagner, "Complementarity of the CERN LEP collider, the Fermilab Tevatron, and the CERN LHC in the search for a light MSSM Higgs boson" Phys Rev. **D62**, 055008 (2000).

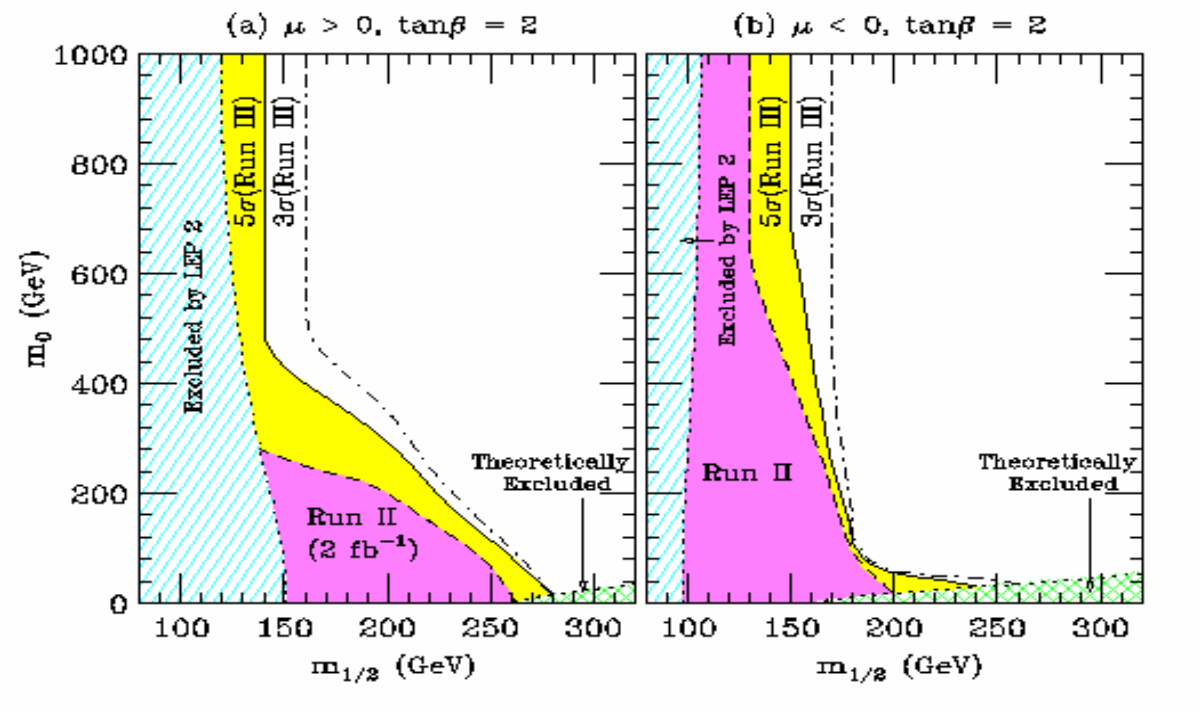

Figure 3 - Contours of 90% C.L. observation at Run IIa, 5σ discovery, and 3σ observation at Run IIb for $p\bar{p} \rightarrow$ SUSY particles $\rightarrow 3l + X$ *in the* $(m_{1/2}, m_0)$ *plane for tan*β*=2, (a)* μ*>0 and (b)* μ*<0.*

Direct searches for squark and gluino production, in jets and missing E_T final states (with or without one or more leptons), have been carried out at the Tevatron since its inception. These still have an important role to play, but once a few inverse femtobarns have been collected, the limits will have reached 400-500 GeV on squark and gluino masses and further improvements will be limited because of the production kinematics. The greatest gains in going from 2 fb^{-1} to 15 fb^{-1} will likely come in searches for lower cross section processes. One of the most promising ways to look for MSSM supersymmetry at the Tevatron is associated chargino-neutralino production: $p\bar{p} \rightarrow \tilde{\chi}_2^0 \tilde{\chi}_1^+; \tilde{\chi}_2^0 \rightarrow l\bar{l}\tilde{\chi}_1^0; \tilde{\chi}_1^+ \rightarrow l^+ \nu \tilde{\chi}_1^0$. This results in a very distinct signature of three leptons and missing energy[4]. Because of its low cross section this search will especially benefit from the increased statistics in Run IIb. The Tevatron's reach in this signature is presented in Figure 3. Note, that Run IIb will not only extend the area of search, but will reach the high m_0 region, which was not accessible before. Good lepton identification and the ability to trigger on low p_T leptons is of great importance for this channel.

The supersymmetric partners of top and bottom quarks – *stop and sbottom* - are often predicted to be lighter then other supersymmetric particles[5]. These particles will be produced strongly in $p\bar{p}$ collisions and thus are likely targets for supersymmetric searches. Decay products include

[4] S. Abel *et al*., "Report of the SUGRA working group for Run II of the Tevatron", hep-ph/0003154.
[5] R. Demina, J. Lykken, K. Matchev, A. Nomerotski, " Stop and Sbottom searches in Run II of the Fermilab Tevatron", Phys. Rev. **D62**, 035011 (2000).

b-jets, and searches will require b-tagging. The pseudorapidity distribution of charged tracks produced in decays of these supersymmetric particles is very similar to that of Higgs decay products, as shown in Figure 4 for two distinctly different kinematic cases with very low energy jets in the final state (b) and with very high energy jets (c). In both cases the b-jets fall within the acceptance of the silicon tracker.

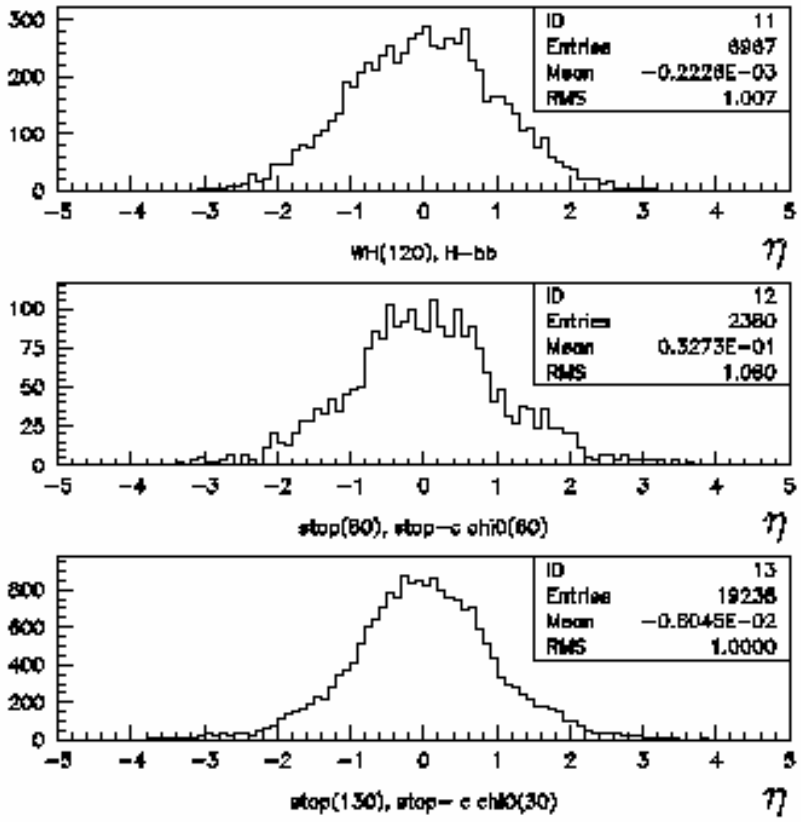

Figure 4 - Pseudorapidity distribution of charged tracks in
a) WH events (M(H)=120GeV/c²);
(b) light supersymmetric top decaying to charm and heavy neutralino
$(M(\tilde{t}) = 80GeV/c^2; M(\tilde{\chi}_1^0) = 60GeV/c^2)$ *;*
c) heavy supersymmetric top decaying to charm and light neutralino
$(M(\tilde{t}) = 130GeV/c^2; M(\tilde{\chi}_1^0) = 30GeV/c^2)$.

Gauge-mediated supersymmetric models predict signatures rich in photons[6]. Interest in these models was sparked by the CDF observation of an $e"e"\gamma\gamma \not\!\!E_T$ event[7]. Though no other events

[6] R. Culbertson *et al*., "Low scale and gauge mediated supersymmetry breaking at the Fermilab Tevatron Run II", hep-ph/0008070.

[7] CDF collaboration (F. Abe *et al*.), "Searches for new physics in diphoton events in $p\bar{p}$ collisions at $\sqrt{s} = 1.8$ TeV, Phys Rev. **D59**, 092002 (1999).

have been found, photonic signatures are worth investigating in Run IIb. The phenomenology of extra dimensions also predicts signatures rich in photons[8].

Alternatives to SUSY are strong dynamics models, for example technicolor or topcolor. Technicolor models predict the existence of technibosons decaying to heavy flavor and gauge bosons[9], e.g. $p\bar{p} \to W\pi_T, \pi_T \to b\bar{b}$. Such searches give vector boson plus heavy-flavor-jets signatures, just like the Higgs search, and will benefit from the detector optimizations motivated by Higgs signatures. More recent topcolor models[10] emphasize non-standard behavior of the top quark and thus could be detected indirectly with thorough studies of top quark properties, or directly through observation of anomalous tb production or production of non-standard Higgs-like bosons decaying to heavy flavor jets.

[8] T. Rizzo "Indirect collider tests for large extra dimensions", hep-ph/9910255.
[9] E. Eichten, K. Lane and J. Womersley, "Finding Low-Scale Technicolor at Hadron Colliders", Phys. Lett. **B 405,** 305 (1997).
[10] C. Hill, "Topcolor assisted Technicolor", Phys. Rev. **D49**, 4454 (1994).

4 STANDARD MODEL PHYSICS

The searches for new particles will be complemented by precision measurements of the quanta of the standard model, which provide indirect constraints on new physics, and which will provide the detailed understanding of backgrounds that discoveries will require.

The Tevatron is entering a new era for top quark physics. Greatly increased statistics will be combined, in DØ, with much improved signal sample purity made possible by silicon vertex b-tagging. We anticipate significant improvements in the precision of the top quark mass measurement, which should reach a level of ~2 GeV with 2 fb^{-1}. The additional statistics of Run IIb should allow a precision of ~1 GeV. Single top production (through the electroweak coupling of the top) has never been observed. Measurement of the cross section would allow the CKM matrix element $|V_{tb}|$ to be extracted. With 2 fb^{-1}, the cross section can likely be measured at the 20% level, allowing $|V_{tb}|$ to be extracted with a precision of 12%. With 15 fb^{-1}, this uncertainty could be roughly halved. The signatures for top pair and single top production involve vector bosons and heavy flavor jets, just like the SM Higgs. They must be understood in detail for the Higgs search and they will benefit from the detector upgrade.

Precision measurements of the properties of the weak boson will continue to be an important part of the Tevatron program. The W-mass precision should reach 30 MeV per experiment with 2fb^{-1} and 15-20 MeV may be achievable with 15 fb^{-1} (theoretical uncertainties are a big unknown in this extrapolation). A W-mass measurement δm_W = 20 MeV combined with a top mass measurement δm_t = 2 GeV will be sufficient to constrain the Higgs mass between roughly 0.7 and 1.5 times its central value[11]. For a 100 GeV best fit, the upper limit of 150 GeV would be well within the Tevatron's region of sensitivity. Such a comparison between direct and indirect Higgs mass measurements would be very interesting whether or not a Higgs signal is seen, as shown in Figure 5.

[11] M. Grünewald et al., hep-ph/0111217 (2001).

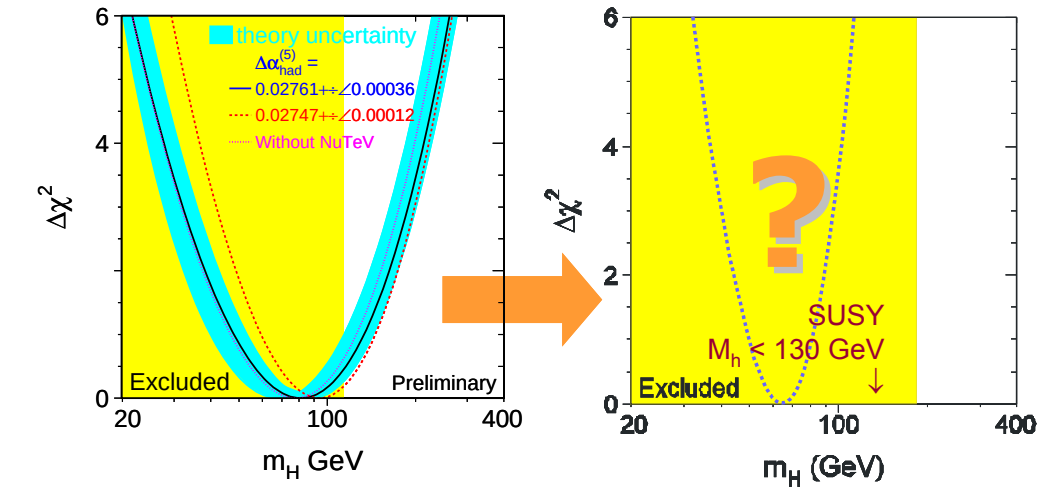

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Figure 5 - Higgs exclusion regions from direct searches (yellow region) confronting indirect constraints from electroweak parameters, top and W mass measurements(blue parabola). The plot on the left is the present situation (summer 2002) and the plot on the right shows a putative future situation including Run IIb results.

Tests of QCD are important at the Tevatron, both as "engineering" measurements and as probes of strong interaction physics. In the former category, measurements of jet production have reached new levels of precision in Run I and are forcing a significant overhaul of the parton distribution functions used in hadron colliders, because the errors on these pdf's must henceforth be treated rigorously. Tevatron jet data from Run II will likely provide strong constraints on pdf's and will be an important input to the global fits. In the latter category, many QCD processes have relatively low cross sections and will benefit greatly from increased datasets available in Run II. Examples are jet production at high-x (jet E_T above about 400 GeV) where the behavior of the cross section is still somewhat uncertain; vector boson plus jet processes, which may be used to determine the strong coupling constant; and diphoton production, which is an important background to Higgs searches at the LHC. In Run I, DØ accumulated about 200 $\gamma\gamma$ candidates. This will increase to 4000 with 2 fb^{-1}, which is still not a huge number, and to 30,000 with 15 fb^{-1} of integrated luminosity.

While the DØ detector is not strongly optimized for b-physics, it possesses a number of features that allow it to make significant contributions in this area. As one example, the low-p_T muon triggering and $J/\psi \rightarrow$ ee triggers will allow a competitive measurement of sin 2β in $B \rightarrow J/\psi\ K_S$ events. With 2 fb^{-1}, sin 2β could be determined to ± 0.07; 15fb^{-1} would reduce this uncertainty by almost a factor of three. Of course, the b-physics program will have to operate within a trigger menu that is constrained by the need to cover the high p_T physics priorities of the experiment.

5 SUMMARY OF PHYSICS OBJECTIVES

The DØ Run IIb upgrade is optimized for Higgs boson observation in the $110<M_H<180 GeV/c^2$ mass region. A low-mass Higgs boson decays predominantly to $b\bar{b}$, and thus efficient b-tagging is of paramount importance to Higgs boson searches. Trigger upgrades that allow the efficient recording of Higgs events are also crucial elements of the upgrade. Lepton identification, crucial for much of the Run IIb physics program, requires efficient triggering and tracking of high p_T tracks in a high occupancy environment, in conjunction with the excellent muon and calorimeter of the DØ detector. $Ht\bar{t}$ production puts additional, more stringent, constraints on efficient tracking and secondary and tertiary vertex reconstruction.

It is clear that the entire DØ physics menu of searches, top quark physics, electroweak measurements, QCD, and even b-physics, will benefit from Run IIb. The upgraded tracker will ensure efficient tracking in a high occupancy environment, the upgraded trigger will allow the required data samples to be recorded with high efficiency, and efficient heavy flavor tagging will be a key ingredient for final states with b and c-quark jets.

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DØ Run IIb Upgrade
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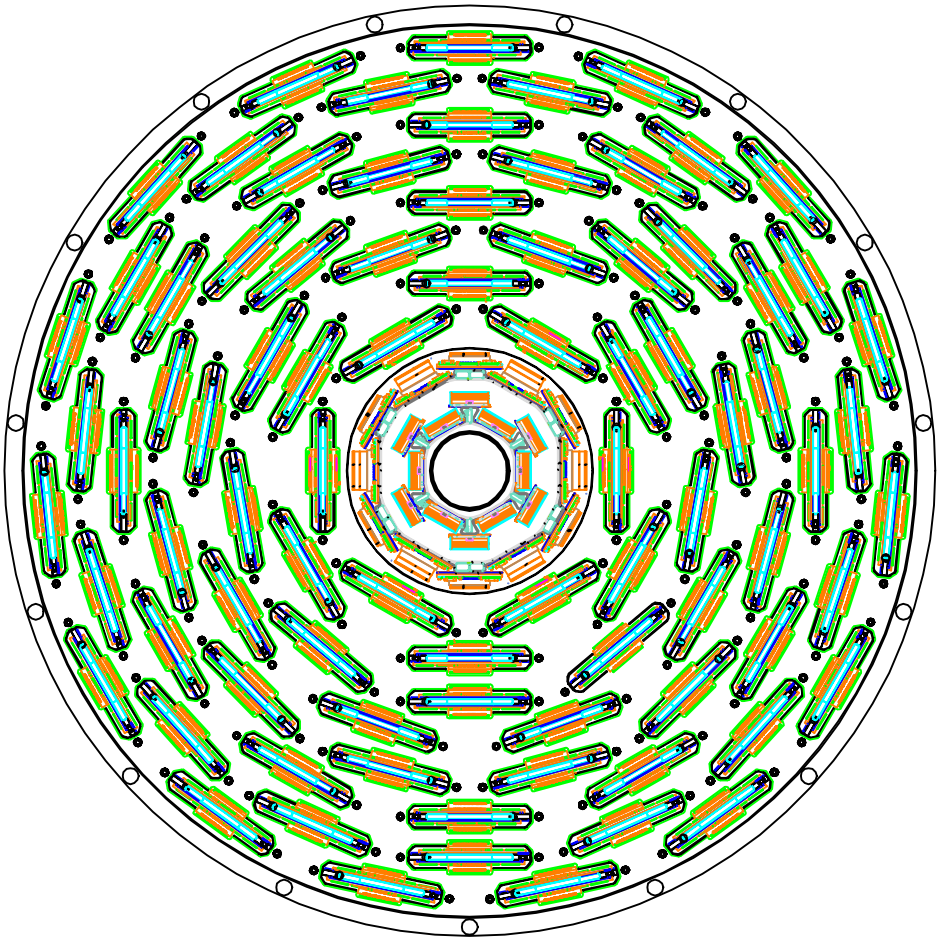

SILICON DETECTOR

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SILICON DETECTOR CONTENTS

1 INTRODUCTION

The current DØ silicon tracker was built to withstand the 2 – 4 fb^{-1} of integrated luminosity originally projected for Run II. Because of the tantalizing physics prospects a higher integrated luminosity brings, the laboratory supports extended running of the Tevatron collider, called Run IIb, which would deliver a total integrated luminosity of 15 fb^{-1} over the course of the full Run II. However, the higher integrated luminosity now scheduled for Run IIb will render the inner layers of the present silicon tracker inoperable due to radiation damage. Of particular importance to be able to exploit the physics potential of the Tevatron is the construction of a replacement of the silicon detector in approximately three years with minimal Tevatron down time. The DØ collaboration carefully studied two options for a Run IIb silicon tracker replacement: "partial replacement" and "full replacement." In the partial replacement option, the present tracker design is retained and the inner two silicon layers are replaced with new radiation tolerant detectors. In the full replacement option, the entire Run IIa silicon tracker is replaced with a new device. An internal review of these two options identified significant risks with the partial replacement option. These include the risk of damage to the components not being replaced, the long down-time required to retrofit the existing detector, an inadequate supply of the SVX2 readout chips, difficulties in adequately cooling the inner layers, and marginal radiation hardness for the extended operation of Run IIb in the layers not being replaced. Furthermore, it is nearly impossible to re-optimize the detector for the Run IIb physics program with the partial replacement option. For these reasons, DØ decided to proceed with the full replacement option for Run IIb and build a new silicon tracker that is optimized for the Higgs search and other high-p_T physics processes.

The design studies for the new silicon detector were carried out within a set of boundary conditions set by the Laboratory and derived from the physics goals for Run IIb. The first requirement imposed is that the detector be able to withstand an integrated luminosity of 15 fb^{-1}. For 15 fb^{-1}, combining the data of both the CDF and DØ detectors, a 5σ discovery of the Standard Model Higgs can be made for a Higgs mass of 115 GeV, a >3σ signal is expected for most of the mass range up to 175 GeV, and Higgs masses up to 180 GeV can be excluded if there is no sign of the Higgs. This result depends crucially on the ability to efficiently tag b-jets, which drives the detector design towards placing the silicon detectors at relatively small distances from the beam. Collecting 15 fb^{-1} of integrated luminosity with a tracking device so close to the interaction point puts stringent requirements on the cooling for the inner layers, and has led to a natural division of the detector into two radial groups: an inner group and an outer group. The laboratory has required that the shutdown for replacement of the current silicon detectors should occur in the year 2005 and should not exceed six months in duration. This timeframe is set by the startup of the LHC collider at CERN. This stringent timetable forces the detector to be replaced in the DØ collision hall. A rollout of the detector, out of the collision hall into the assembly hall, replacing the silicon detector, and rolling it back in is an operation estimated to take at least nine months and would risk further damage and delay. Installation of the new silicon detector in the collision hall constrains the installable package length to 52", determined by the space available between the central and end calorimeters in the collision hall which is only 39". The last requirement imposed by the Laboratory is that the project should be completed within a tightly constrained budget. To reduce the cost and to keep to the schedule, as much of the present data acquisition system as possible will be retained. Even though there are

significant boundary conditions, the new detector presented in this document is designed to have better performance than the Run IIa detector and is expected to be completed within the allocated time, calling for an installation in the summer of 2005.

This report describes the current conceptual design of the new silicon detector for the DØ experiment for Run IIb. Section 2 gives an overview of the proposed DØ silicon detector design and serves as an introduction to the following sections. Section 3 discusses the silicon sensors, Section 4 the mechanical aspects of the design, and Section 5 the readout electronics. Section 6 describes the production and testing, Section 7 describes temperature and radiation monitoring, and Section 8 describes the software needed for the quality assurance and testing of the devices. Section 9 presents the results of simulation studies to determine the expected detector performance and Section 10 summarizes the silicon part of the TDR.

2 SILICON DETECTOR DESIGN

2.1 Introduction

The silicon detector project is introduced in this section. The design is based on an optimization of the physics performance of the detector while at the same time satisfying various boundary conditions, both external and internal. The external boundary conditions come from the anticipated accelerator performance in Run IIb. Interfacing the new detector within the existing framework, notably the trigger framework, sets internal constraints. Moreover, building on our experience constructing the Run IIa silicon detector, fabrication and assembly methods proposed for the new silicon detector were reevaluated and the strategy adopted for Run IIb should result in a much more efficient construction cycle. The new detector, for example, will employ only single-sided silicon technology. The remainder of this section will describe the basic design features of the proposed silicon detector.

2.2 Design Constraints

2.2.1 Tevatron parameters

The DØ Run IIb TDR describes a silicon detector designed to operate at a luminosity of 5×10^{32} cm^{-2} sec^{-1} with 132 ns bunch spacing and a small crossing angle. At this luminosity, an average of 5 minimum bias interactions will accompany the high-p_T interaction of interest. The laboratory has recently changed the baseline plan for Run IIb operations to a luminosity of 2×10^{32} cm^{-2} sec^{-1} with 396 ns bunch spacing and no crossing angle. Luminosity leveling will be used to hold the luminosity at 2×10^{32} cm^{-2} sec^{-1} and the achievable integrated luminosity is expected to be the same as if there were no leveling and an initial luminosity of about 3.4×10^{32} cm^{-2} sec^{-1}. This mode of operation also yields an average of 5 minimum bias interactions accompany the high-p_T interaction. Thus, detector performance should be nearly identical for these two operating modes except for the difference in crossing angle. For 396 ns bunch spacing, the absence of a crossing angle leads to a larger longitudinal spread in the luminous region, with 5% of the interaction vertices occurring outside the 96 cm fiducial length of the innermost silicon layers. This loss in geometrical acceptance is not included in the detector studies presented below.

2.2.2 Radiation environment

The collaboration embarked on radiation studies of silicon sensors for both the present and proposed Run IIb detector to determine the timescale within which the present detector would become inoperable and to determine the operating parameters for the new detector. The leakage currents and depletion voltages were measured using 8 GeV protons from the booster facility at Fermilab up to a dose of 15 MRad. The measurements agree with others made outside of DØ and will be described in the next section. Based on these measurements, and parameters obtained by other experiments, simulation studies were carried out of the leakage current, depletion voltage, and equivalent noise to determine the silicon operating temperature and to ensure that the device can withstand the foreseen accumulated dose. The design operating

temperature of the inner layer was chosen to be –10 degrees Celsius. We also determined that a minimum radius of about 18 mm for the innermost layer of silicon will allow for an adequate safety margin for running the detector to integrated luminosities of 15 fb^{-1}.

2.2.3 Silicon track trigger

The Run IIa silicon detector employs a Silicon Track Trigger (STT) that processes data from the Level 1 Central Track Trigger (CTT) and the silicon tracker. It associates hits in the silicon with tracks found by the Level 1 CTT. These hits are then fit together with the Level 1 CTT information, thus improving the resolution in momentum and impact parameter, and the rejection of fake tracks. The STT has three types of electronics modules:

- The Fiber Road Card (FRC), which receives the data from CTT and fans them out to the other modules.

- The Silicon Trigger Card (STC), which receives the raw data from the silicon tracker front end. It processes the data to find clusters of hit strips that are associated with the tracks found by the CTT. Each card accepts input from at most eight readout hybrids.

- The Track Fit Card (TFC), which fits a trajectory to the CTT tracks and the silicon clusters associated with it. These results are relayed to the Level 2 Central Track Trigger. Each card can accept at most eight STC inputs.

The trigger observes a 6-fold ϕ-symmetry. The STT modules are located in 6 VME crates, each serving two 30-degree azimuthal sectors. Currently each of these crates holds one FRC, nine STCs, and two TFCs - one per 30-degree sector. Each crate can hold at most 12 STCs, with a possibility to go to 16 STC cards with a redesigned backplane. It is these constraints, combined with the 6-fold symmetry that has to be observed for the new silicon detector, which severely limits the parameter space for the geometry of the tracker.

The data from the silicon tracker must be channeled into the TFC cards such that all hits from a track are contained in one TFC. In layers 0, 1, and 2 overlaps between adjacent sensors are large enough so that each sensor can be uniquely associated with one TFC. This divides the detector into 12 azimuthal sectors. To maintain full acceptance for tracks with p_T>1.5 GeV/c and impact parameter < 2 mm, the data from some sensors in layers 3, 4, and 5 must be channeled into two TFCs, which are in some cases located in different crates. These constraints have resulted in a geometry with 12-fold symmetry for layers 0 through 2, and an 18-, 24- and 30-fold geometry for layers 3, 4 and 5, respectively.

2.2.4 Cable plant

The total number of readout modules in the new system is constrained by the currently available cable plant, which allows for about 940 cables. The present Run IIa detector has 912 readout modules. The cable plant is limited due to space constraints. There simply is not enough space between the central and end calorimeters to route more cables. Only replacing the full cable plant would allow an increase in the number of cables, but this is cost prohibitive. Given that the new detector has more silicon sensors, this implies that not every sensor can be read out and that

an adequate ganging scheme will have to be implemented. An elegant solution using double-ended hybrids has been found which is described in the next section.

2.3 Baseline Design Overview

The proposed silicon detector has a 6 layer geometry arranged in a barrel design. The detector will be built in two independent barrel assemblies joined at z=0. The six layers, numbered 0 through 5, are divided in two radial groups. The inner group, consisting of layers 0 and 1, will have axial readout only. Driven by the stringent constraints on cooling, these layers will be grouped into one mechanical unit called the inner barrel. These layers have a significantly reduced radius relative to the current tracker. Given the tight space constraints, emphasis has been placed on improving the impact parameter resolution. The outer group is comprised of layers 2 through 5. Each outer layer will have axial and stereo readout. The outer layers are also important for providing stand-alone silicon tracking with acceptable momentum resolution in the region $1.7 < |\eta| < 2.0$ where DØ has good muon and electron coverage but lacks coverage in the fiber tracker. The outer layers are assembled in a mechanical unit called the outer barrel. The inner barrel is inserted into the outer barrel forming a barrel assembly. A barrel assembly is the basic unit that is installed in the collision hall. While all 6 layers are designed to withstand 15 fb^{-1} of integrated luminosity with adequate margin, separating the inner layers into a separate radial group provides a path for possible replacement of these layers. The outer layers should easily withstand luminosities up to ~25 fb^{-1}. The inner two layers with axial readout will provide an adequate impact parameter resolution for tagging of b-jets. Two layers as close to the interaction point as possible are preferred to efficiently tag b-jets. The remaining space can accommodate at most four axial-stereo layers, which is adequate to do the pattern recognition. Hence our design calls for six layers.

Of paramount importance to the successful construction of the new detector in the less than 3 years available, is a simple modular design with a minimum number of part types. This is one of the reasons that single-sided silicon sensors are used throughout the detector. Only three types of sensors are foreseen: highly radiation tolerant sensors for layers 0 and 1, with two sizes to best fit the geometrical constraints, and a single sensor size for the four outer layers. All of the sensors are envisioned to have axial traces with intermediate strips. The stereo readout in the outer layers will be accomplished by tilting the sensor slightly with respect to the beam axis.

Figure 1 shows an axial view of the Run IIb silicon tracker. The emphasis is on obtaining improved impact parameter resolution in the R-ϕ plane while maintaining good pattern recognition. The inner two layers have 12-fold crenellated geometry and will be mounted on a carbon fiber support structure. Figure 2 shows an axial view of these two inner layers. Layer 0 will have its innermost sensor located at a radius of about 18.6 mm. These sensors will be two-chip wide, 78.4mm long with 50 micron readout pitch and intermediate strips. The pitch is chosen to obtain the best impact parameter resolution possible using conventional technology. Given the size of the luminous region, 6 sensors in z are used in each barrel assembly.

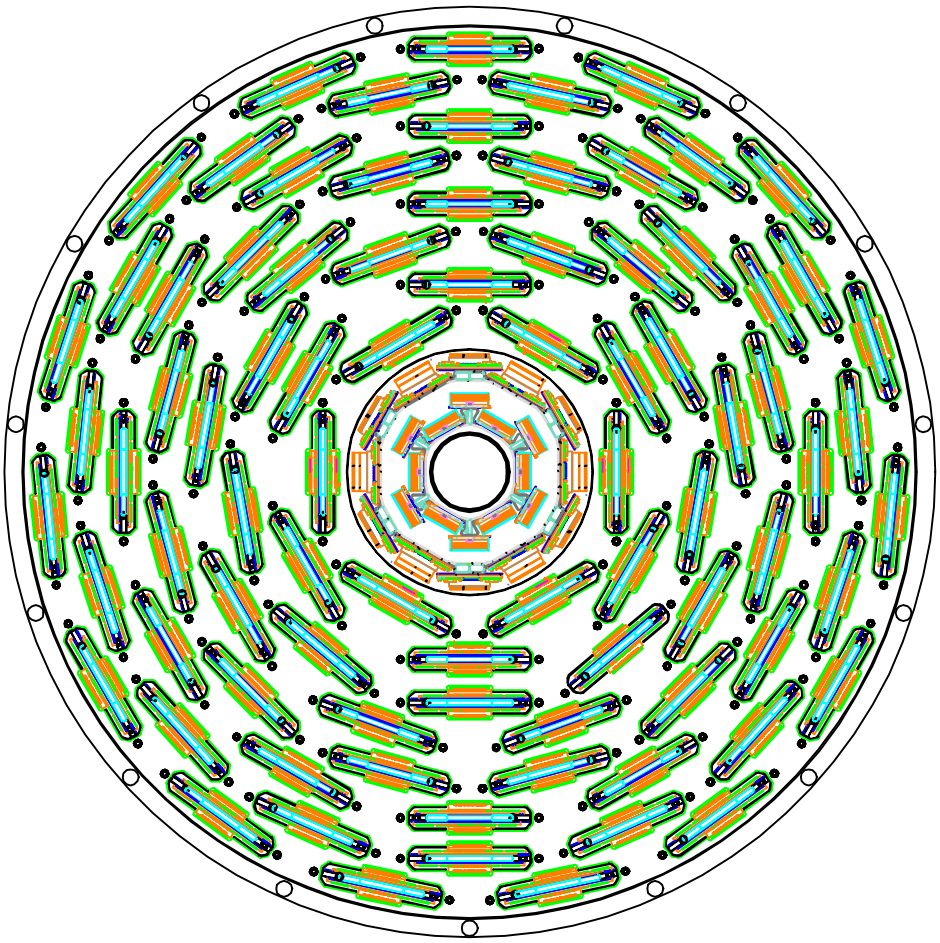

Figure 1 - Axial view of the proposed tracker upgrade. The outer four layers provide both axial and stereo track measurements, while the inner two layers only provide axial track measurements.

Because of the lack of space available, the cooling requirements for the innermost layer, and to minimize the amount of material, no readout electronics will be mounted on the sensors, i.e. the layer will have 'off-board' electronics. Analog cables will be wirebonded to the sensors, carrying the analog signals to a hybrid where the signals will be digitized and sent to the data acquisition system. Keeping the hybrid mass out of the detector active region also helps in reducing photon conversions. Present CDF experience with noise issues from these cables are a concern but given the requirement that the inner layer has to survive 15 fb^{-1}, there is no alternative to off-board readout electronics. A major challenge in building the mechanical structure for this layer is ensuring that it provides the cooling capability needed to maintain the silicon at a temperature of –10 degrees C while fitting in all the components necessary and keeping mass to a minimum so that the impact parameter resolution is not degraded. The sensor breakdown voltages are specified to be >700V. The bias system for the inner layers will be designed to deliver voltages up to 1000V.

Layer 1 will contain 3-chip wide sensors, 79.4mm long with 58 micron readout pitch, with intermediate strips. The geometry matches the segmentation of Layer 0. Because Layer 1 will also sustain substantial radiation doses, the cooling requirement is an average temperature of –5

degrees C, while the bias voltage supply requirements will be the same as for Layer 0. Although the heat load from putting hybrids directly on the sensors is greatly increased (0.5 Watts per readout chip), noise and production considerations have led to on-board electronics for all layers except Layer 0.

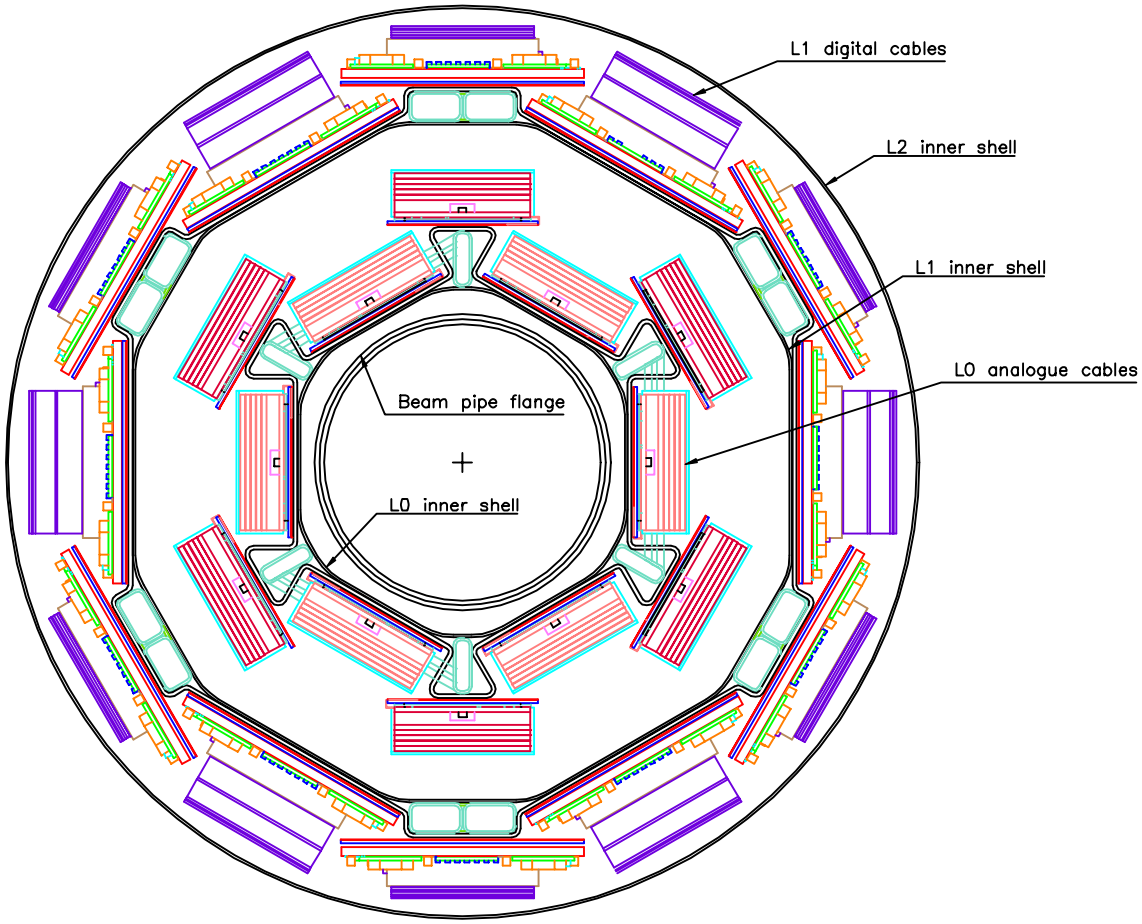

Figure 2- Axial view of Layers 0 and 1 within the sensor active region. The silicon sensors are mounted on a carbon-fiber support structure with inboard cooling tubes. The readout uses analog low mass cables which connect to hybrids outside of the active region.

In Layers 2-5 only one type of sensor will be used. The sensors will be 5 chips wide, 100mm long with 60 micron readout pitch and intermediate strips. This pitch allows for direct bonding between SVX chips and the sensors and retaining the fine resolution in Layer 5 significantly improves pattern recognition. These layers employ stiff stave support structures. A stave will have an inner core that will carry the cooling lines. Silicon will be mounted on the core; on one side there will be axial readout and on the other small-angle stereo. The stereo angle will be obtained by rotating the sensors. The design allows for a depletion voltage of >300V for these outer layers. Recall that the detector is built in two halves, north and south; each stave will thus cover a half-length in z.

The longitudinal segmentation is driven by the need to match η coverage throughout the detector up to η=2, by the desire to minimize the number of different elements in the design, and by observing the constraint to stay within the existing cable plant. For Layer 1 six sensors, each 79.4mm long, form one half length in z, matching the coverage for L0 which is in the same mechanical structure. Staves consisting of six 100mm long sensors are used in layers 2-5. Figure 3 shows a plan view of the tracker inside the fiber tracker.

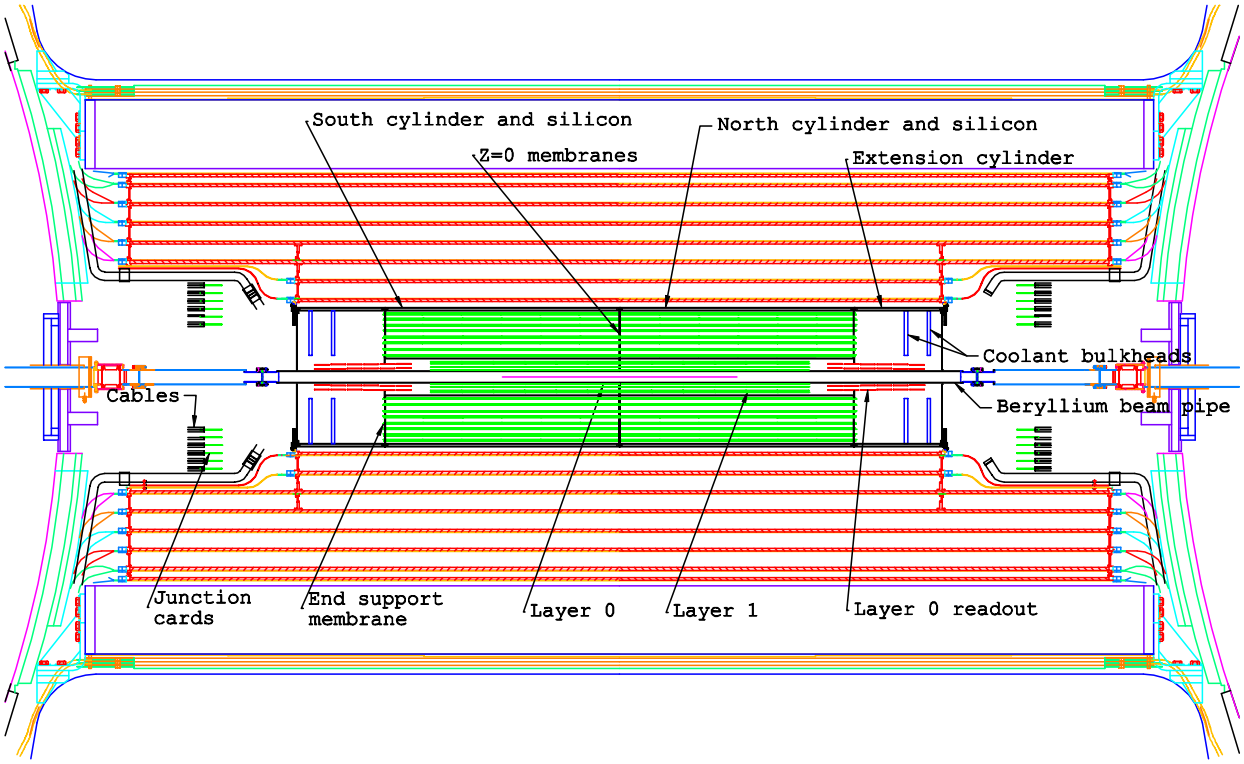

Figure 3 - Plan view of the Run IIb silicon tracker inside of the fiber tracker.

The total number of readout modules in the new system is constrained by the currently available cable plant, which allows for about 940 readouts. The present Run IIa detector has 912 readout modules. This implies that not every one of the 2304 sensors in the detector can be read out separately. By studying deadtime it was determined that for Layers 2 and higher we are able to read out a total of 10 chips. This allows us to use a double-ended hybrid design that reduces the hybrid readout count by a factor of two. A double-ended hybrid services two readout segments at once. Since the sensors are 5-chip wide for the outer layers, the double-ended hybrids will readout 10 chips at a time. The digital signals are carried out of the tracking volume using a digital cable that connects to the hybrid. Layer 1 also employs the double-ended hybrid concept. Since sensors are 3-chip wide in Layer 1, a hybrid will read out 6 chips at a time.

Using double-ended hybrids we have reduced the hybrid count significantly, but not enough to satisfy our cable number constraint. Occupancy studies and confused hit probabilities were used to determine how best to longitudinally combine (gang) sensors to form a readout segment in z.

These studies are described in DØ Note 3911 [1]. For the inner two layers every sensor is read out separately. For Layers 2-5 we have a total of 6 sensors per half module in z. Here the two innermost sensors are read out individually. The outermost 4 sensors are ganged together such that each of 2 sensors is wirebonded together to make one readout unit. This arrangement is depicted in Figure 4. Each stave thus has four hybrids, with each hybrid servicing two readout segments, two for the axial readout and two for the stereo readout. The modules are indicated by the length (in cm) of the two readout segments. A hybrid with 10 cm sensors on each side of the hybrid is called a 10/10 module while one with 20cm readout on either end of the hybrid is referred to as a 20/20 module. Figure 5 shows the longitudinal segmentation for all layers. An 'S' indicates single sensor readout, and '1/2D' indicates a readout segment serviced by one side of a double-ended hybrid.

Figure 4 - Readout configuration for outer layer staves. The upper configuration is for the axial side of the stave, the lower shows the stereo side of the stave. The interaction point (z=0) is at the far right-hand side of the drawing

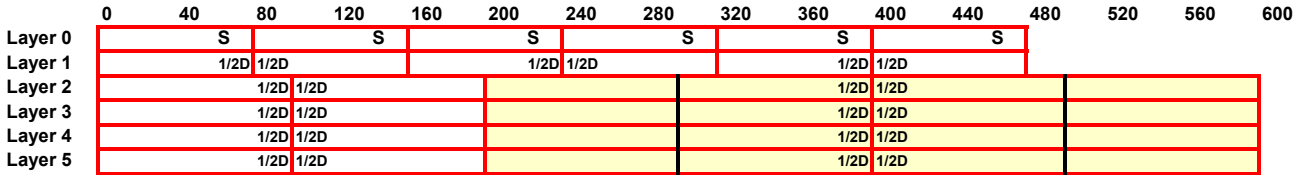

Figure 5 – Longitudinal segmentation of the detector. The top row is a ruler showing the length (in mm) for each of the layers in the detector. .

For the stereo side of the stave we have chosen to use the maximum stereo angle possible given the mechanical constraints. This allows us to obtain the best r-z resolution possible. Studies of confused hits, ghost tracks, and occupancy indicate that it is best for the pattern recognition to have the traces of ganged sensors line up, so as to make one long 20 cm trace. For the 10 cm readout segments the maximum stereo angle is 2.48 degrees while for the 20 cm segments the maximum stereo angle is 1.24 degrees. We then end up with 4 types of modules for the outer layers: 10/10 Axial and Stereo and 20/20 Axial and Stereo modules.

[1] DØ Note 3911, "MCFAST Studies of the Run IIb Silicon Tracker", R. Lipton and L. Stutte, October 4, 2001.

The decision was made in November 2000 to read out the new silicon system using the SVX4 chip. Both CDF and DØ will use this chip. This chip is based on the SVX3 chip, but will be produced in 0.25 micron technology. This chip is intrinsically radiation hard and is expected to be able to withstand the radiation doses incurred in the innermost layers. In order not to have to redesign the entire DØ data acquisition and trigger system, the SVX4 chip will be read out in SVX2 mode. The SVX2 chip is the readout chip for the Run IIa detector and incurs deadtime on every readout cycle unlike the SVX3 chip that can run in a deadtimeless mode. As the readout chip is a joint project with both CDF and DØ, there is a premium on employing the same hybrid technology so that the design work can be shared. We plan to use ceramic hybrids using beryllia. No pitch adapters will be needed in the DØ design so that the SVX4 chips will be wirebonded directly to the silicon sensors for layers 1-5.

The digital signals will be launched onto a jumper cable from the hybrid through an AVX connector. These flex cables will run on the top and bottom of the stave to a junction card located at the end of the active region on a bulkhead. There will be one junction card per stave. That is, each junction card will service four hybrids, the two hybrids from the axial readout and the two hybrids from the stereo readout. The junction card is a passive element and simply carries the signals from the digital cable to a twisted-pair cable. The twisted-pair cables run to the adapter cards that are mounted on the face of the calorimeter. The adapter card will interface to the existing data acquisition system. The adapter card has two new functions in Run IIb. First, it will convert 5V lines to 2.5V, necessary for operating the SVX4 chip. The current data acquisition system uses the SVX2 chip, in which the lines are single-ended. The SVX4 chip will be run differentially at 2.5V. The adapter cards will convert the single-ended lines to differential lines. From the adapter card downstream, it is anticipated that we can retain the full data acquisition system as is. Some modifications will be needed for the interface boards that pass the voltages to the detector to allow for higher voltages for the biases for the inner layers, but no major modifications are foreseen.

The design parameters are summarized in Table 1. There are a total of 2304 silicon sensors in this design, read out with 888 hybrids containing 7440 SVX4 chips. In layers 2-5 there will be a total of 168 staves, containing 336 readout modules. For comparison, the Run IIa silicon detector has 793K readout channels while the Run IIb one will have 952K readout channels. The Run IIb silicon detector is designed to allow for faster construction due to fewer and simpler parts than the Run IIa device. Comparisons between the detectors show that the major difference between the two detectors is found at the inner and outer radii. Figure 6 shows axial views of both detectors drawn to scale. By decreasing the radius of the innermost layer from 25.7 mm to 18 mm, the impact parameter resolution is improved by a factor of 1.5. Because we are removing the F-disks and the entire cable plant from the Run IIa barrel modules, we are able to utilize this space at larger radii for silicon sensors. The increase from 94.3mm to 163.6mm for the outer radius allows us to put in two more layers of tracking necessary for the pattern recognition in the Run IIb environment. With the new detector we will have better stand-alone silicon tracking. A number of factors affect the tracker performance, and consequently the physics performance, of the detector. Among these factors are tracker acceptance, amount of material, resolution, and pattern recognition capabilities. We have optimized our design to the extent possible to obtain a detector that is superior to the Run IIa detector and that will allow us to be well placed for the possibility of discovering new physics.

Table 1. Design Parameters. There are a total of 2304 sensors and 888 hybrids in this design.

Layer	Nphi	R(mm) Axial	R(mm) Stereo	# Sensors in z	# Sensors Total	Sensor Width (mm)	Readout Pitch (μm)	# Readout in z	# Chips per Readout	Chips Total	# Hybrids Total
0A	12	17.95	--	12	72	15.50	50	12	2	144	72
0B	12	24.80	--	12	72	15.50	50	12	2	144	72
1A	12	34.75	--	12	72	24.97	58	12	3	216	36
1B	12	39.00	--	12	72	24.97	58	12	3	216	36
2A	12	54.57	57.43	12	144	40.34	60	8	5	480	48
2B	12	70.04	72.90	12	144	40.34	60	8	5	480	48
3A	18	89.45	86.59	12	216	40.34	60	8	5	720	72
3B	18	103.67	100.81	12	216	40.34	60	8	5	720	72
4A	24	116.52	119.38	12	288	40.34	60	8	5	960	96
4B	24	130.48	133.35	12	288	40.34	60	8	5	960	96
5A	30	148.83	145.97	12	360	40.34	60	8	5	1200	120
5B	30	162.75	159.75	12	360	40.34	60	8	5	1200	120
Total					**2304**					**7440**	**888**

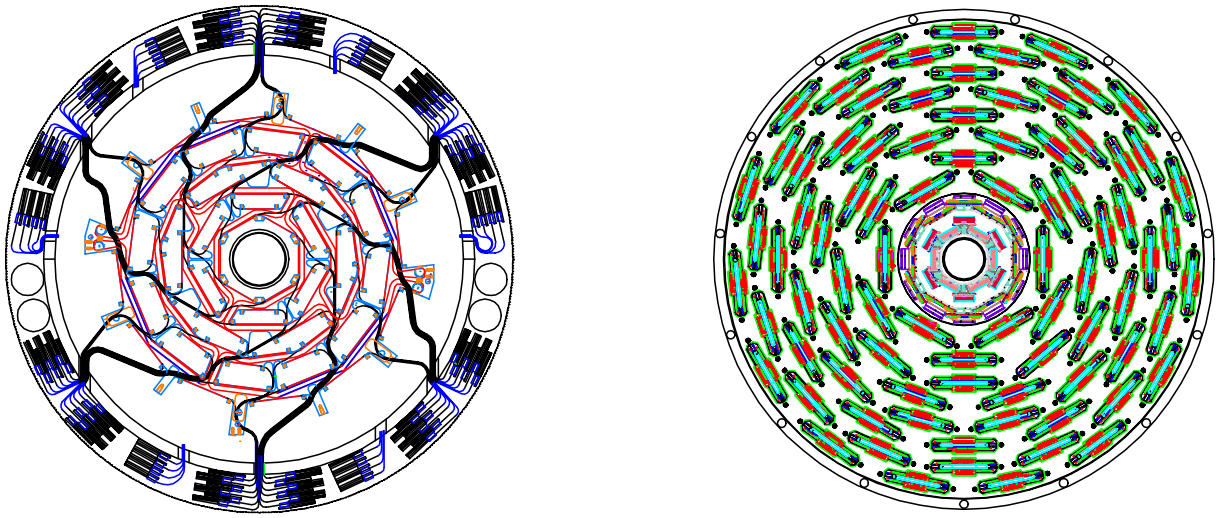

Figure 6 - Comparison of the axial views of the Run IIa and Run IIb silicon detectors. The left picture shows the Run IIa detector whose innermost layer resides at a radius of 25.7mm. The innermost layer of the Run IIb detector resides at a radius of about 18 mm.

3 SILICON SENSORS

3.1 Introduction

The main requirements for the silicon detector are: efficient and reliable tracking, precise vertex measurement, and radiation hardness. As described above, this is achieved with a 6-layer device. The four outer layers are constructed of 60 μm readout pitch silicon sensors and provide hits essential for pattern recognition in a high-occupancy environment. In addition, two inner layers (layer 0 and 1), constructed with 50/58 μm readout pitch silicon sensors with intermediate strips at 25/29 μm, provide precise coordinate measurement essential for good secondary vertex separation. Reliable operation of silicon sensors in a high-radiation environment is critical to the experiment's success. Over the operating period, the inner layers of the Run IIb silicon detector will be subject to a fluence of about 2×10^{14} equivalent 1 MeV neutrons per cm^2. We were guided in our design and technology choice by our experience in Run IIa detector construction as well as by recent research and development in the radiation hard technology.

3.1.1 Lessons from Run IIa

Several difficulties were encountered by DØ during the Run IIa silicon detector prototyping and construction. The gained Run IIa experiences and important conclusions are:

- Sophisticated double-sided silicon sensors were difficult to produce and lead to lower yield and hence significant delays. Single-sided sensors however, which have been produced both by Elma for the H-disks and Micron for the 1st and 3rd layers of barrels 1 and 6 for the Run IIa detector, had higher yields and caused much less trouble due to their simplicity.

- The introduction of an alternative vendor at the later stages helped to speed up production.

- The large number of sensor types complicated the production process.

- Double-sided sensors proved to be very difficult to handle.

- Radiation studies have shown that double-sided (and especially 90^o double-metal) silicon sensors have limited radiation hardness (more details in "Radiation testing")

- Detailed pattern recognition studies have shown that in high occupancy environment, "ghost" hits produced in 90^o sensors lead to a significant fraction of fake tracks and increased reconstruction time.

For the Run IIb silicon sensors, we adopted the following guidelines:

- Use only single sided silicon sensors.

- Try to identify alternative vendors whenever possible.

- Limit the number of sensor types to 3.
- Use only small stereo angles, achieved by sensor rotation.
- Avoid double metallization.

In our choice of radiation hard technology we have benefited greatly from radiation hard silicon R&D studies motivated primarily by the needs of LHC experiments.

3.1.2 Radiation damage in silicon

The most important damage mechanism in silicon is the bulk damage due to the non-ionizing part of the energy loss, which leads to a displacement of the silicon atoms in their lattice. It causes changes in doping concentration (and, eventually, silicon type inversion), increased leakage current, and decreased charge collection efficiency. Surface damage due to ionizing radiation results in charge trapping at the surface interfaces and leads to increased interstrip capacitance and electronics noise. A general overview of radiation damage in silicon detectors can be found in DØ Note 3803.

The change in the effective impurity or doping concentration $N_{eff} = [2\varepsilon\varepsilon_0/(ed^2)]\cdot V_{depl}$ measured as a function of the particle fluence for n-type starting material shows a decrease until the donor concentration equals the acceptor concentration or until the depletion voltage V_{depl} is almost zero, indicating *intrinsic* material. Towards higher fluences the effective concentration starts to increase again and shows a linear rise of acceptor like defects. The phenomena of changing from n-type to p-type like material has been confirmed by many experimental groups and usually the detector is said to have undergone a "type inversion" from n-type to p-type. The change of the effective doping concentration can be parameterized as

$$N_{eff}(\Phi) = N_{D,0} \cdot \exp(-c_D\Phi) - g_c\Phi$$

where the first term describes donor removal from the starting donor concentration $N_{D,0}$ and g_c indicates the rate of the radiation induced acceptor state increase. Hence donor removal happens exponentially whereas acceptor states are created linearly with fluence. Type inversion for standard n-type material with resistivity $\rho\approx 5k\Omega cm$ typically occurs at a fluence of about $(1\text{-}2)\times 10^{13} cm^{-2}$.

The radiation-induced changes of the doping concentration are initially not stable and exhibit two main components with different time behaviors and temperature dependences. With time constants in the range of a few days a decrease in the radiation induced changes occurs soon after irradiation. This effect is called short-term annealing or beneficial annealing, because it mitigates the acceptor creation and hence the type inversion process. However, at room temperature an increase in the acceptor states appears after about two weeks of annealing leading to even higher depletion voltages. This long term or reverse annealing is a major concern because of its limiting factor for long-term operation of silicon detectors in high fluence regions. Reverse annealing can be almost completely suppressed by cooling the detector to 0^oC or less and by minimizing the maintenance periods of the silicon detectors at room temperature.

For the operation of detectors the control of leakage current is important in two aspects, one is the resulting higher shot noise, the other is the increased bulk heat production in silicon which may lead to a thermal runaway if the silicon detector is not properly cooled. The leakage current of silicon detectors increases with radiation dose due to the creation of additional gap states which will lead to more electron-hole pair generation and thus to an increase in bulk or generation current. This generation current is by far the dominant part of the entire leakage current after the silicon has been irradiated. The increase in leakage current can be parameterized as:

$$I = I_0 + \alpha \cdot \Phi \cdot A \cdot d$$

Where I_0 is the bias current before radiation, α is a damage rate coefficient usually defined at T=20°C and dependent on particle type, Φ is the particle fluence given in particles per cm^2, A is the detector area, and d is the thickness of the detector. The exact value of α depends on particle type and energy and varies between (2-3) $\times 10^{-17}$ A/cm once the silicon is completely annealed and α reaches a constant value. The leakage current rises linearly with fluence and does not depend on either the silicon detector properties or special process characteristics during the silicon sensor manufacturing. The leakage current in silicon sensors due to generation of electron-hole pairs is strongly temperature dependent and the ratio of currents at two temperatures T1 and T2 is given by

$$I_2(T_2) / I_1(T_1) = (T_2/T_1)^2 \cdot \exp(-[E_g(T_1-T_2)]/[2\kappa_b T_1 \cdot T_2])$$

With κ_b being the Boltzmann constant ($\kappa_b = 8.6\times10^{-5}$ *e*V/K) and E_g the gap energy in silicon (E_g = 1.2*e*V).

A third effect from radiation is the reduced charge collection efficiency. The primary mechanism leading to a decrease in the collection of electrons or holes is charge trapping at defect sites, i.e. a decrease of the carrier lifetime with increasing fluence. In addition surface damage in the silicon oxide due to ionizing radiation results in the creation of fixed positive charge at the surface boundary between silicon and silicon oxide. This leads to increased interstrip capacitances and, therefore, higher electronic noise.

Seriously damaged detectors will require high bias voltages to operate efficiently. The deteriorated charge collection can be efficiently recovered by applying a bias exceeding the depletion voltage. This overbiasing also reduces to normal values the increased interstrip capacitance due to the surface charge accumulation. High voltage operation is therefore crucial for radiation hard silicon and the breakdown voltage of the device will determine the limits of survivability.

3.1.3 Radiation hard designs

The CMS collaboration designed single-sided 300 μm thick n-type sensors, which were reliably working after heavy irradiation at bias voltages up to 500 V[2]. The main features of the design are p+ strips in n-bulk silicon, which are biased with polysilicon resistors and are AC coupled to the readout electronics. The front side of the detector (with p+ strips) has a peripheral n+ implantation (n-well) at the edge and is followed by a p+ single guard ring structure to prevent junction breakdowns. This guard ring design has been optimized in cooperation with Hamamatsu and is also successfully implemented with other producers. It is proven to be radiation hard and CDF is using this type of sensors for the L00 of SVX in Run IIa. Other radiation hard designs reduce the risk of an early breakdown at the edges of the silicon by including a multi-guard ring structure[3].

We note here that in the case of AC-coupled double-sided sensors (as presently used by CDF and DØ in Run IIa) the high bias voltage is applied across the coupling capacitor on one of the sides (unless the electronics is floating at the same potential). Together with considerably higher costs related to the double-sided wafer processing, the requirement that AC capacitors hold off the bias voltage is a strong limitation for the double-sided detectors and we are not considering using them for the upgrade.

Another option to improve the radiation hardness at moderate fluences is the use of low-resistivity silicon as an initial detector material[4]. Low bulk resistivity of silicon corresponds to high depletion voltage of the device. For example, a 300 μm thick detector with bulk resistivity of $\rho \approx 1.0 k\Omega \cdot cm$ depletes at $V_{depl} \approx 300\,\mathrm{V}$. High initial depletion voltage values shift the type-inversion point towards higher fluences, and limits the depletion voltage growth after the type inversion, thus improving the radiation hardness of the sensor in the moderate fluence regime of up to 10^{14} cm^{-2}.

A new technological development driven by the R&D work of the ROSE collaboration[5] uses oxygenated silicon materials to improve the radiation hardness of silicon detectors. Oxygen concentrations ($[O_i] \approx 10^{17} cm^{-3}$) in silicon considerably improves the radiation hardness of the detector for charged particle fluence and effectively lowers the needed bias voltage for radiation damaged detectors. No improvement was observed for damage caused by neutrons. The charged particle component is expected to dominate (for example at CMS only 1/10th of the damage is accounted for by neutrons). There are indications also that the reverse annealing saturates at high fluences for oxygen enriched silicon.

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[2] S. Braibant et al., Investigation of design parameters for radiation hard silicon, Nucl.Instr.Meth A485:343-361,2002.
[3] A. Bischoff et al., Breakdown protection and long term stabilization for Si-detectors, Nucl. Instr. & Meths. **A326** (1993)27-37.
[4] RD20 collaboration, "Radiation damage studies of field plate and p-stop n-side silicon microstrip detectors", Nucl. Instr. & Meths. **A362** (1995) 297-314, 1995.
[5] Rose Collaboration, Nucl. Instr. & Meth. in Phys. Res. **A466** (2001) 308-326

High oxygen concentrations reduce the donor (n-impurity) removal rate significantly and can mitigate the acceptor (p-impurity) creation. The simplest way to enrich silicon material with oxygen is a diffusion process in the $\sim 1200^{o} C$ oxygen atmosphere of a quartz oven. This technology is easy and economic and has been successfully transferred to a number of silicon detector vendors.

Finally there is an alternative to use n+ strips on n type silicon. It has been shown that they offer a better charge collection efficiency at under-depleted voltages and, therefore, would improve the performance after irradiation. However, the detectors technologically are more complicated and require further R&D efforts. Since for $n^{+}n$ sensors certain techniques like p-stop or p-spray are necessary to maintain the strip isolation, the detectors are becoming more and more complex which would considerably drive up the costs. Furthermore, it is not clear that such a fine pitch structure of 25μm we are requiring for layer 0 is technologically feasible on $n^{+}n$ devices. Except LHCb, which is pursuing a $n^{+}n$ option for its vertex microstrip detector, neither of the other LHC silicon strip detectors will use $n^{+}n$ and we are considering this technology as too risky for the tight Run IIb schedule.

In summary, three approaches have been successfully explored so far:

- Special designed guard ring structures. Such guard rings are important in order to keep the breakdown voltage before and after irradiation as high as possible.

- Low-resistivity silicon sensors. Increasing initial donor concentration leads to type inversion after higher radiation doses, thus slowing the radiation damage.

- Oxygenated silicon. Controlled increase in oxygen concentration slows down the growth of depletion voltage with irradiation dose.

It is possible to combine all three approaches. The techniques have been transferred to multiple silicon vendors.

3.2 Silicon Sensors for Run IIb

For the construction of the Silicon Microstrip Tracker for Run IIb DØ we propose the use of AC-coupled, single-sided single-metal p^{+} on n-bulk silicon devices with integrated polysilicon resistors as baseline sensors. Only bias resistors based on polysilicon are capable of sustaining the high radiation level the Run IIb detector will experience. Either a multiguard structure (see Figure 7a) or a single guard ring structure with a peripheral n-well at the scribing edge (see Figure 7b), developed in cooperation with Hamamatsu's design engineers, is necessary to allow operation at high bias voltages.

a) b)

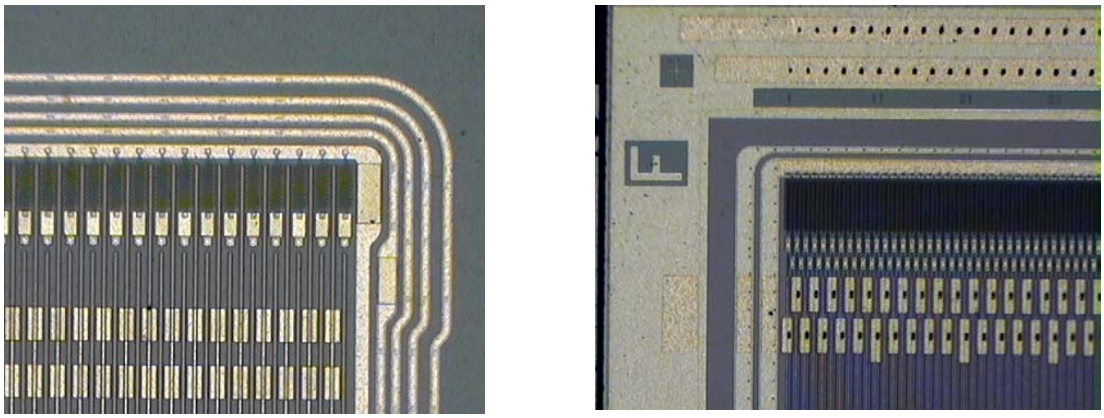


Figure 7 a) Multiguard ring structure of ELMA prototype sensors. b) Hamamatsu's sensor with a single guard ring structure and a peripheral n-well.

We prefer a silicon microstrip vendor capable of doing multilayered dielectric substrates for the coupling capacitors for two reasons. First, it will significantly reduce the number of pinholes and therefore shorted capacitors in the detector. Secondly, by using silicon nitride (Si_3N_4) in addition to silicon oxide, the coupling capacitor value can be increased while leaving the thickness of the dielectric substrate constant.

Oxygenation is considered as a serious option for the inner layers 0 and 1 in order to improve the radiation hardness further.

DØ envisions using 3 sensor types for Run IIb. Their geometric parameters are summarized in Table 2.

Table 2 Geometric parameters of silicon sensors.

Layers	Active Length (mm)	Active Width (mm)	Strip pitch /readout pitch (μm)	# readout channels	# of sensors + spares
0	77.36	12.8	25/50	256	144+50%=216
1	77.36	22.272	29/58	384	144+50%=216
2-5	98.33	38.372	30/60	639	1896+20%=2280

All outer layers are constructed from sensors of the same type. In the specified geometry, two such sensors can fit on one 6" silicon wafer. Unfortunately, 6" technology is not widely used among companies capable of producing silicon sensors. Hamamatsu, ST Microelectronics, SINTEF and Micron Semiconductors are the only vendors which have implemented 6" technology successfully so far. We have contacted all of the mentioned vendors above and

believe that only Hamamatsu and ST Microelectronics are able to produce the amount and quality we require for the Run IIb detector at decent costs. Since ST Microelectronics is presently processing only 6''-wafers with a thickness of 500μm, the number of potential vendors is reduced to one company: Hamamatsu. The other vendors, which could manufacture silicon strip sensors, continue to produce sensors using 4" or even 5'' technology. Although it would be possible to modify the design to use two 50-mm long sensors to fit on a 4" wafer, instead of one 100-mm long sensor, this choice has many drawbacks: increased number of parts; additional wire bonding and sensor testing load; increased dead area; and, most importantly, significant increase in cost.

Upon our request, the company ST Microelectronics is currently evaluating if their 5''-wafer production line is suited for the fabrication of fine pitch microstrip silicon detectors in the wafer thickness we are requesting. One L2-L5 sensor would fit on a 5''-wafer. However, we have to wait for the outcome of the evaluation study at ST, in order to understand if ST could be considered as an additional potential vendor.

We have chosen to use sensors with an active length of 77.36 mm for layers 1 and 0 to minimize occupancy and noise, and more importantly, to take advantage of a wider choice of vendors. These sensors can be fabricated with two L0 type sensors or one L1 type sensor on a single 4" wafer. Since these sensors will be subject to a very harsh radiation environment, it is critical to choose a vendor that can provide radiation-resilient devices.

Table 3 The main specifications for layer 0 and 1 and the outer layers 2-5.

Specifications:	**Layer 0/1**	**Layer 2-5**
Wafer thickness	320±20μm, wafer warp less than 50μm	320±20μm, wafer warp less than 50μm
Depletion voltage	V<300V	V<300V
Leakage current	<100nA/cm2 at RT and FDV+10%V, total current < 4μA at 700V	<100nA/cm2 at RT and FDV+10%V, total current < 16μA at 350V
Junction breakdown	>700V	>350V
Implant width	7μm	8μm
Al width	2-3 μm overhanging metal	2-3 μm overhanging metal
Coupling capacitance	>10pF/cm	>12pF/cm
Coupling capacitor breakdown	>100V	>100V
Interstrip capacitance	<1.2pF/cm	<1.2pF/cm
Polysilicon bias resistor	0.8±0.3 MΩ	0.8±0.3 MΩ
Not working strips	<1%	<1%

We plan to use intermediate strips in all sensors to improve the single hit resolution. A multiple guard-ring, or alternatively, a Hamamatsu-style single guard-ring structure is necessary to ensure high breakdown voltage after irradiation. The two aforementioned structures occupy roughly a 1-mm wide area on each edge of a silicon sensor. The main parameters of the silicon sensors are given in Table 2 and Table 3.

3.3 Fluence Estimation for Run IIb

Several fluence predictions for Run II have been given by Matthews *et al*[6], Frautschi *et al*.[7] and Ellison *et al*.[8] Leakage current measurements performed on the CDF SVX and SVX' silicon detectors as a function of sensor radius from the beam and delivered luminosity during the Run

[6] John A. J. Matthews et al., CDF Notes 3408 and 3937.
[7] M. Frautschi, CDF Note 2368.
[8] J. Ellison and A. Heinson, "Effects of Radiation Damage on the DØ Silicon Tracker", DØ Note 2679 (July 1995).

Ia+b provide us with a solid basis for expectations. The derived charged particle fluence quantities vary among the various authors between 1.5×10^{13} MIPs/cm^2/fb^{-1} and 1.9×10^{13} MIPs/cm^2/fb^{-1} for the new SVXII layer 0 detectors which are located at a radial distance of r≈2.42cm from the beam axis. All of the mentioned CDF expectations have in common that the radial scaling of the fluence occurs as $r^{-1.68}$, a fact, which has been verified by independent dose measurements in the CDF detector.

To normalize the observed CDF leakage current measurements to a standard neutron or proton fluence, assumptions about the radiation damage rate constant α have to be made. Matthews[9] has given an equivalent 1 MeV neutron fluence per fb^{-1} of $(2.19\pm0.63)\times10^{13}\cdot r[cm]^{-1.68}[cm^{-2}/fb^{-1}]$. In his fluence determination, he assumed a frequently used α value for 1 MeV neutrons in order to convert the observed current increase to an effective 1 MeV neutron fluence. He took α to be $(2.86\pm0.18)\times10^{-17}$ A/cm, which is still a good value for neutrons[10] if most of the annealing of the leakage currents has occurred. Since the CDF strip measurements are not done in a fully annealed state, he applied a factor of 1.1 to α according to common annealing parameterizations[11] in order to take the partial annealing of the detector currents into account. Matthews propagated the uncertainties on silicon temperature, leakage current measurements, and α value into a final fluence uncertainty of ±30%.

The number of secondary particles produced in the Be beam pipes of the CDF and DØ experiment should be rather similar. The only difference may occur in the number of curling particles which are traversing the silicon layers more than once (caused by different magnetic field strengths in each experiment). CDF has a solenoid with 1.4T while DØ has a 2T field for their magnet. In the study of Ellison et al, it was found that 50% of the total fluence will come from looper particles in the DØ magnetic field. Frautschi, who has done similar studies for CDF assumed only a 30% contribution.

The strategy of the predictions for the leakage current rise and depletion voltage changes for Run IIb presented here will be as follows: For the leakage current estimations we are using the measured strip current numbers by CDF in Run I and scale to the appropriate DØ geometries and temperatures. This approach is essentially independent of the α value, but assumes the same fluences of charged particles in the CDF and DØ experiments. In order to estimate the upper uncertainties for the leakage currents, we varied the temperature at which the CDF strip leakage current measurements took place according to their given uncertainties. Furthermore, we then increased the CDF strip currents and hence the fluence by another 20% in order to take into account a possible difference in the numbers of looper particles between DØ and CDF. More details on this approach and on the results can be found in DØ Note 3959.

The proposed 1 MeV equivalent fluence of $(2.19\pm0.63)\times10^{13}\cdot r[cm]^{-1.68}[cm^{-2}/fb^{-1}]$ by Matthews can be translated into an equivalent fluence of any other particle at any kinetic energy by knowing the corresponding so-called non-ionizing energy loss (NIEL) damage or displacement damage cross section value of the particle at a given energy. These NIEL values for neutrons,

[9] J. Matthew et al., CDF Notes 3408 and 3937.
[10] M. Moll, private communication.
[11] R. Wunstorf, Ph.D. Thesis, Hamburg, 1992.

protons, pions and electrons are normalized to the standard displacement damage cross section for 1 MeV neutrons according to an ASTM standard and are tabulated in a useful online compilation[12].

For the depletion voltage predictions, the 1 MeV neutron fluence number as given by Matthews is taken, and under the assumption of the NIEL hypothesis, we calculate the depletion voltage changes according to the latest parameters of the Hamburg model, which gives the best current phenomenological description of the change in effective doping concentration in silicon during hadron irradiation. To obtain an upper bound on the depletion voltage after irradiation, a safety factor of 1.5 (in agreement with CDF) is added and the 1 MeV equivalent fluence is varied accordingly.

3.4 Silicon Sensor Performance Extrapolations for Run IIb

3.4.1 Leakage current and shot noise estimations

Strip leakage current measurements from CDF as a function of sensor radius from the beam and delivered luminosity are used to derive an average increase in the strip currents at T=(24±2)°C which can be scaled from their strip geometry to the DØ configuration as shown in Table 4. The thickness of the silicon sensors is taken to be 320μm. Radial scaling is taken to be $r^{-1.7}$.

The strip leakage currents in nA and per fb^{-1} for the various layers of the DØ Run IIb detectors at five different temperatures, which are of interest for the operation in Run IIb, are given in Table 5. Note that not only a readout strip, which is AC coupled to the preamplifier, but also an intermediate strip produces the same current. Therefore we do not distinguish between the two types of strips if only strip currents are considered. The calculations assume that the silicon sensors generating the leakage currents are held uniformly at the considered temperature. In reality however, the silicon sensors have temperature drops along the silicon length and an attempt to include the temperature gradient along the silicon sensors is given in the next section.

[12] A. Vasilescu and G. Lindstrom, Displacement damage in silicon, online compilation, http://sesam.desy.de/gunnar/Si-dfuncs.html

Table 4 Sensor parameters used to extrapolate Leakage Current and Depletion Voltage Measurements.

Layer	Min. radius (cm)	Max active Length (cm)	Pitch (μm)	Strip Volume (mm^3)
0-A	1.78	7.74	25	0.619
1-A	3.48	7.74	29	0.718
2-A	5.32	19.66	30	1.887
3-A	8.62	19.66	30	1.887
4-A	11.69	19.66	30	1.887
5-A	14.7	19.66	30	1.887

Finally, the shot noise that is caused by the strip leakage currents is obtained in the following way[13]: ENC_{shot} = SQRT(12·I[nA]·τ) electrons Equivalent Noise Charge (ENC) where τ is the shaping time of the amplifier in ns, which is taken to be 132 ns. The shot noise calculations assume that the intermediate strips fully couple their noise through interstrip capacitances to the two neighbor readout strips. For fine-pitch detectors the interstrip capacitance dominates the total strip capacitance. We conservatively assume that the noise of the intermediate strips is fully coupled to the readout strips and do not include the reduction of noise due to coupling to the backplane. The expected strip noise in ENC after 15 fb^{-1} is shown in Table 6, again at different temperatures.

[13] H. Spieler, IEEE Trans. Nucl. Sci. NS-32, 419 (1985)

Table 5 Expected strip leakage currents in nA/fb^{-1}

Layer	T = -10°C	T = -5°C	T = 0°C	T = +5°C	T=+10°C
0A	14.0	23.7	39.4	64.7	104.2
1A	5.2	8.8	14.6	24.0	38.7
2A	6.7	11.3	18.9	31.0	49.8
3A	2.9	5.0	8.3	13.6	21.9
4A	1.7	3.0	4.9	8.1	13.1
5A	1.2	2.0	3.4	5.5	8.9

Table 6 Expected strip noise in ENC after 15 fb^{-1}

Layer	T = -10°C	T = -5°C	T = 0°C	T = +5°C	T=+10°C
0A	814	1061	1370	1753	2225
1A	496	646	834	1068	1355
2A	563	733	947	1212	1539
3A	373	487	628	804	1021
4A	288	376	485	621	788
5A	237	309	399	511	649

The uncertainties in the measured CDF strip currents were 10%. In addition, there is a temperature uncertainty of ±2°C. By changing the operation temperature of SVX and SVX' from T=24°C to T=22°C, our estimate produces higher leakage currents by 15-20%. In addition to the temperature uncertainty of the leakage current measurements, the value itself was increased by 20% to take into account the possibility of different charged particle fluences between DØ and CDF due to the number of curlers in the higher DØ field. Studies using DØ radiation monitors at r=3 cm indicate that this effect is small between 1.5 and 2 Tesla.[14] The combined resulting upper leakage current values are given in the table. This approach should be

[14] Naeem Ahmed, private communication of "Looper Studies" in progress, August 23 2002.

conservative enough to estimate the expected leakage currents and hence the shot noise levels for Run IIb in a safe way.

3.4.2 Leakage currents for a realistic silicon temperature profile

The calculation of the leakage currents and hence shot noise in the previous section assumed a uniform temperature along the silicon sensors. Due to the assembly of the hybrid on top of the silicon sensors, the temperature along the silicon is not constant and large temperature drops in the silicon itself are possible. In a finite-element analysis (FEA) study, the temperature gradient along the silicon sensors has been determined for layer 1 and layer 2 modules based on a realistic modeling of the power dissipation, the heat transfer of the cooling fluid and the thermal impedances. The coolant temperature was set to $T_{coolant}$=-15ºC. The FEA based temperature gradients have been used to estimate an equivalent average temperature T_{equiv} , at which the same leakage current output would have been produced, as if the sensor would have been uniformly kept at this temperature. The Figure 8 shows the anticipated temperature distribution along the z-axis for a layer 2 module. The strip leakage currents are in nA/fb^{-1} normalized to a strip unit length of 3 mm (used as binning in the FEA) and are shown as well. Since the stave design is identical in the other outer layers, the same thermal profile is expected for layers 3-5.

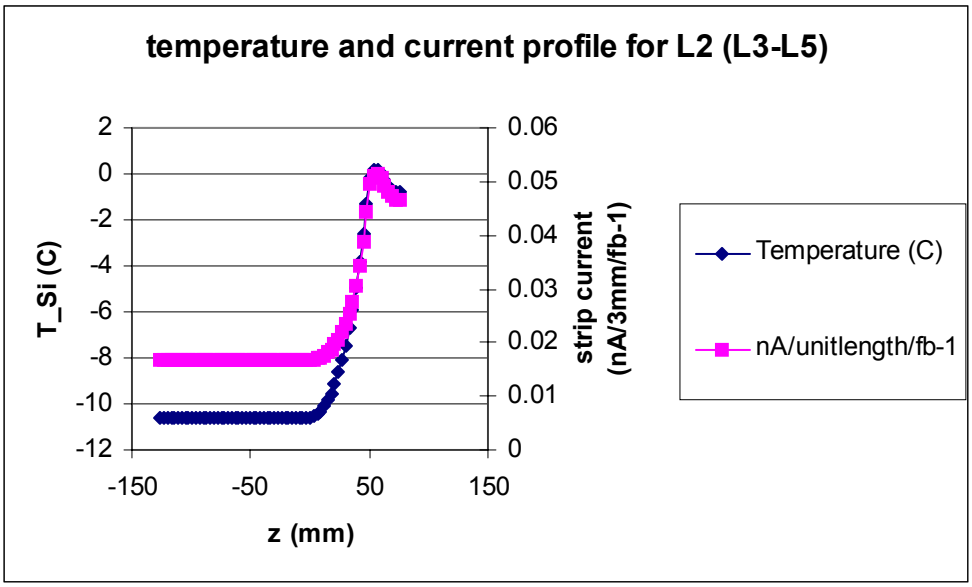


Figure 8. Expected temperature gradient and strip currents in nA per unit length (3mm) and per fb^{-1} as a function of z. The temperature profile has been obtained by FEA.

The warmest region of T~0ºC in the silicon sensor is, where the readout chips on the hybrid are located. To obtain the total strip currents for the layers, the differential strip currents along the ladder modules have been summed. Based on the produced currents of the assumed temperature profile of the silicon, the equivalent temperature T_{equiv} for a long module – if kept at uniform temperature – would be T_{equiv}=-8ºC. This reference temperature is valid for a coolant at $T_{coolant}$=-15ºC and can be used to estimate the leakage current values, which are tabulated in Table 5. In another FEA study the thermal performance of the layer 1 design has been addressed in order to

obtain the corresponding layer 1 thermal profile. In that case, we found the layer 1 equivalent temperature to be T_{equiv}=-5ºC, if the coolant is circulated at $T_{coolant}$=-15ºC.

3.4.3 Depletion voltage predictions

As previously mentioned, the depletion voltage predictions we are presenting are based on the 1 MeV equivalent fluence assumptions for Run II by Matthews *et al*. In addition we apply a safety factor of 1.5 to that fluence. The latest parameters for the stable damage constants, the beneficial annealing and the reverse annealing constants of the so-called Hamburg model have been used along with the Tevatron running scenario listed in Table 7. The obtained depletion voltage predictions are called standard depletion voltage predictions.

Table 7: The Tevatron Run IIb running scenario used for the calculation of the depletion voltage changes.

Year	Max luminosity pb-1/week	Shutdown (months)	max luminosity fb-1/year	Cumulated luminosity fb-1
2005	61	4	1.81	1.81
2006	81	1	3.38	5.19
2007	81	1	3.85	9.04
2008	81	1	3.85	12.89

.

In the standard predictions, it is assumed that the silicon detector is kept cold entirely during the luminosity runs as well as during the shutdown periods. This operation temperature is assumed to be uniform. The resulting standard depletion voltage for different operating temperature for the layers 0, 1 and layer 2 are shown in Figure 9. We present three calculations for layer 0 at uniform silicon temperatures of –10ºC, 0ºC and +10ºC and with a starting depletion voltage of 150V as well as one scenario for layer 0 with starting depletion voltage of 50V. Furthermore, we give two standard depletion voltage predictions for layer 1 and one prediction for layer 2.

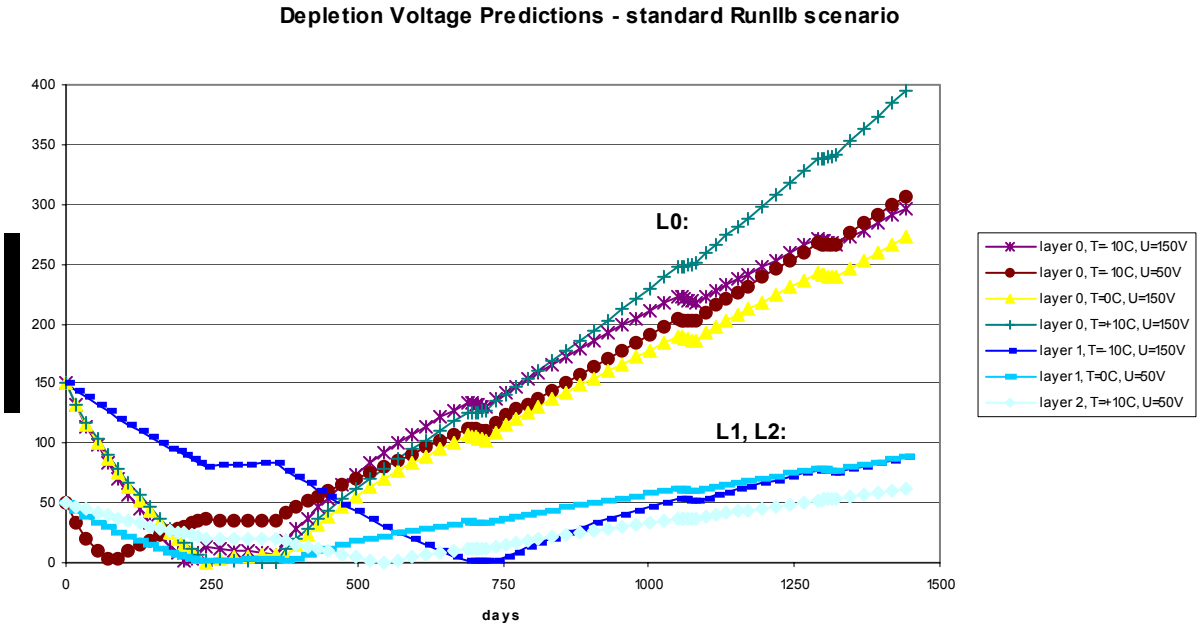


Figure 9. - Depletion voltage for layer 0 and layer 1 sensors as a function of days in Run IIb. The running scenario is given in table5. The 1460 days of running correspond to an integrated luminosity of 12.9 fb-1.

In the standard Run IIb scenario, the depletion voltage of layer 0 will reach values of around 300V as long as the silicon temperature does not exceed T=0ºC. Estimates show that it does not really matter for the final depletion voltage if the initial depletion voltage happens to be around 150V or only 50V. Layer 1 is expected to deplete at around 100V at the end of the standard running period. It is surprising that the final depletion voltage of layer 1 is the same for two presented calculations using very different assumptions: T=-10ºC and U_{depl}=150V compared to T=0ºC and U_{depl}=50V. This can be explained by a suppression of the reverse annealing term even at T=0ºC. Indeed, a calculation (not shown in the figure) having layer 1 at T=+10ºC would reach a final depletion voltage of 140V and hence shows the first signs of reverse annealing effects, which now begin to dominate over the beneficial annealing mechanism. Finally, Figure 9 contains a depletion voltage prediction for layer 2, which depletes below 80V at the end of the standard running. This value is obtained even at a moderately high temperature of T=+10ºC.

Note, that these values represent only the value of the depletion voltage itself and do not guarantee full charge collection in the silicon. A safety margin of at least a factor of 1.5 in the bias voltage should be applied in order to have enough flexibility in overbiasing the detectors and to compensate potential charge losses due to ballistic deficits after irradiation. Therefore, we have specified the breakdown voltage of the layer 0 sensors to be above 700V to provide for such a safety margin.

There is some variation in the radiation damage constants and reverse annealing parameters used in the Hamburg model for different silicon wafer materials. However, these uncertainties are absorbed in the fluence safety factor of 1.5, which we have included in the depletion voltage

calculations. Moreover, we feel that it is important to irradiate samples of detectors used in Run IIb to verify that the damage response is consistent with an operation of up to 15MRad, corresponding to more than twice the expected dose of layer 0 in Run IIb.

As it was demonstrated in Figure 9, temperature effects of the reverse annealing in the standard running scenario tend to saturate already at T=0ºC, and the depletion voltage values for T= 0ºC and T=-10ºC did not differ much. However, reverse annealing increases rapidly if the operation temperature reaches higher temperatures of T=+10ºC or more. At such high temperatures the reverse annealing makes a significant contribution and cannot be neglected anymore. This could be a concern for the detector operation if a warming up period due to cooling problems or simply an access at room temperature happens. In addition we have to investigate the operation of our silicon sensors if the radiation levels are higher than expected or if the Tevatron running extends over the standard scenario. Therefore we have expanded the standard Run IIb scenario now over a total of 6 years and calculate the anticipated depletion voltage after having accumulated a total luminosity of 20 fb^{-1}. Moreover, periods at room temperature have been included in this scenario.

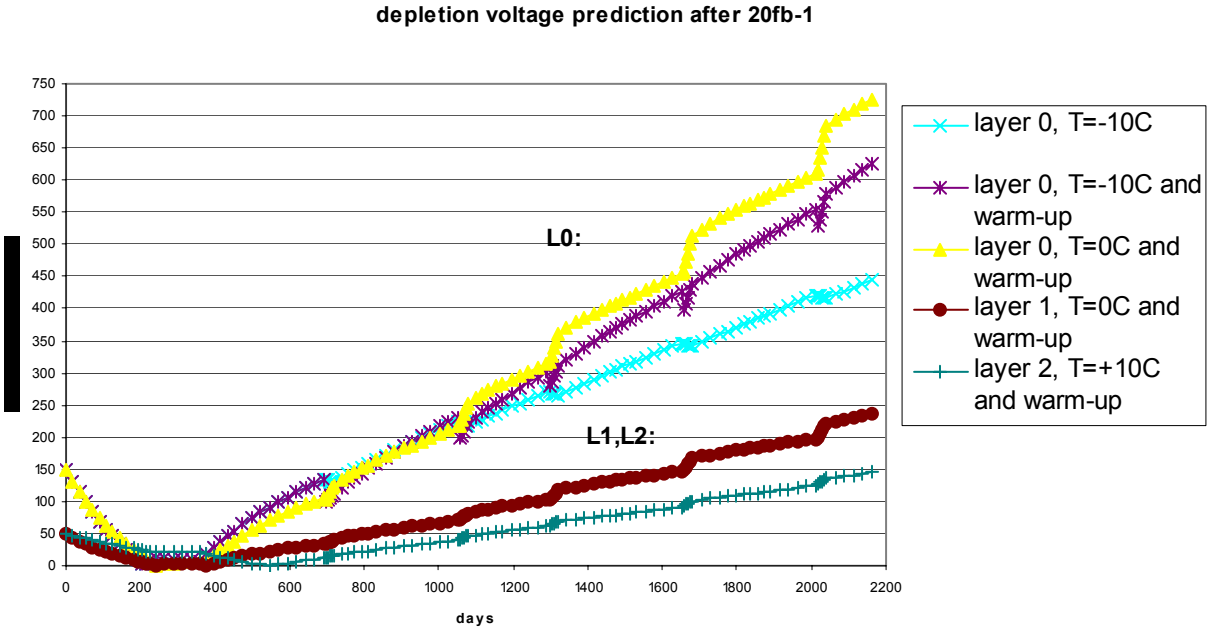


Figure 10. Depletion voltage prediction after 20 fb^{-1}.

Figure 10 contains such depletion voltage graphs for layer 0, 1 and 2. In this extended scenario the layer 0 sensors are expected to deplete now at around 450V (without warming up) and since we are specifying the sensor breakdown to be at least 700V, we would still have enough margin in the biasing to accommodate a longer Tevatron running of up to 20fb^{-1}.

In addition this plot contains two other layer 0 depletion voltage graphs: Four warm periods, each lasting 4 weeks at room temperature are included, in order to estimate the reverse annealing effects. One calculation was done keeping the sensors normally at T=-10ºC and the other one at

T=0ºC. The reverse annealing will now dominate and will shift the depletion voltage to much higher levels of around 700V. It is therefore quite important to avoid any warm up after the detector has been irradiated. We should point out, that for the operation of the silicon detectors in layer 0 and 1, a temperature as cold as possible is safer against reverse annealing, especially if warm periods are included in the depletion voltage scenario.

3.4.4 Signal to noise ratio

Signal to noise ratio (S/N) is an important parameter that ultimately limits the detector lifetime. Based on previous studies and CDF experience in Run 1, S/N starts affecting b-tagging efficiency seriously when it degrades below a value of 5 [15]. Our design goal is to keep the S/N conservatively above 10 for all layers of the detector. The S/N should remain above this limit even for an extended Run IIb of up to 20fb^{-1}. In addition we prefer to set the operation temperatures such, that the S/N of the silicon layers should not degrade by more than 15% over the course of the Run IIb period in order to ensure a stable and robust S/N over the full lifetime of the silicon detector.

In our signal-to-noise (S/N) estimates we assume that sensors can be fully depleted and that one MIP produces a most probable charge value of 23,000 e$^-$ in 320 μm silicon. We have considered several contributions to the total noise:

- Noise in the front end due to capacitive load: the analog cable in layer 0 contributes with 0.4 pF/cm to the total capacitive load. The silicon sensors are conservatively assumed to have a total load capacitance of 1.4pF/cm, dominated by the interstrip capacitance. The ENC noise behavior of the front end chip (SVX4) is taken to be 450+43*C(pF) according to the specifications.

- Noise due to the series resistance of the aluminum traces of the silicon sensors and – for layer 0- the copper traces of the analog cable. The serial noise varies between ~210e for layer 1 sensors (only 7.66cm long) and ~780e for 19.7 cm long modules in layer 2-5.

- Shot noise from detector leakage current as calculated before. A shaping time of 132 ns is assumed

- Thermal noise due to the finite value of the bias resistor (~250e).

[15] J. Albert et al. " The relationship between signal-to-noise ratio and b-tag efficiency." CDF Note #3338.

In the following, we will present the expected signal to noise ratio based on the noise input assumptions mentioned above as a function of luminosity for layer 0, layer 1 and layer 2 and 3. We plot the S/N for different temperatures in order to derive temperature bounds for the operation of the various layers.

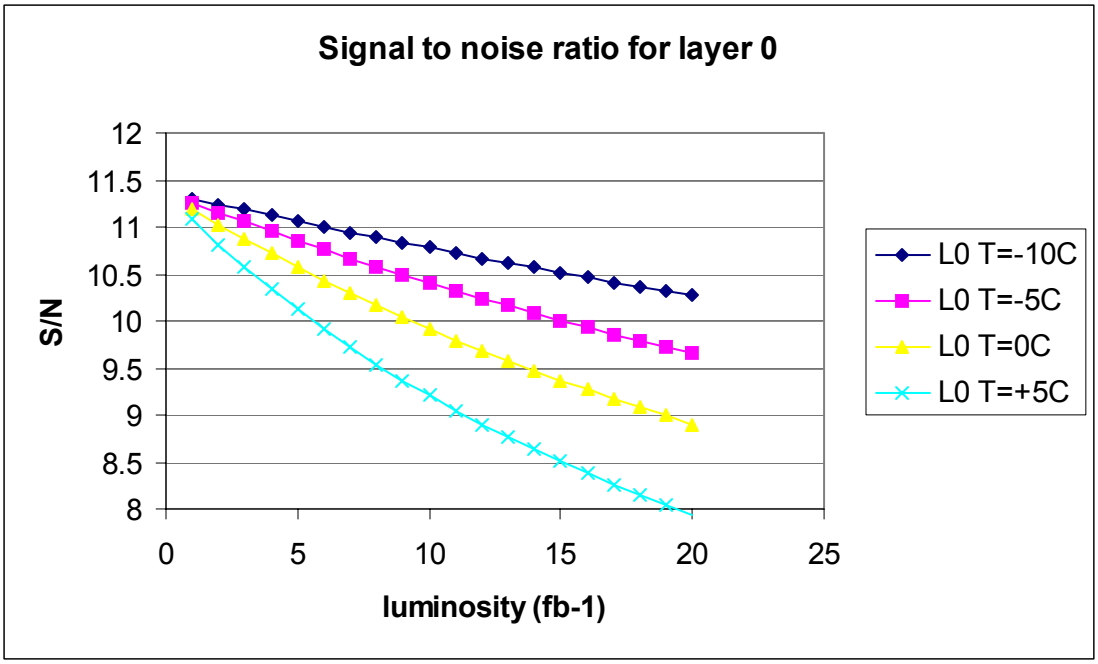


Figure 11. - Signal to noise ratio for layer 0 modules as a function of luminosity for different running temperatures. The noise expected from the analog cable is included.

Figure 11 shows the S/N behavior as a function of luminosity for layer 0 modules. This innermost layer is a special case since is has an up to 450 mm long analog cable to route the silicon signals to the hybrids. These cables will be designed to have a maximum capacitance of not more than ~20 pF[16] so that the total capacitive load of the silicon ladder including the analog cable can be kept around 30 pF. Due to this large load capacitance and serial resistance of the cable, the S/N will be not much higher than 11:1 and any further degradation by additional shot noise should be carefully avoided. Therefore, the best strategy would be to keep the detectors in the innermost layer as cold as possible, i.e. at a temperature of T=-10°C. The S/N will then remain larger than 10 even after 20 fb^{-1}. It is therefore very important to provide the cooling for this layer such that silicon temperatures of T=-10ºC can be reached at the end of the running period. This will give additional safety margin against reverse annealing in case of warming up periods.

Generally, a much higher S/N is achieved with modules from layer 1 due to the absence of the analog cable and the short module length. The S/N of layer 1 is visible in Figure 12. A very high and robust S/N of more than 19:1 can be maintained if layer 1 is kept at T=-5C or lower during

[16] K. Hanagaki, DØ Note 3944

the complete Run IIb period. Under such conditions the S/N performance loss due to the radiation induced shot noise increase is mitigated to less than 15%.

The detectors in layer 2-5 represent with a maximum active length of 19.66 cm a total capacitive load of almost 28 pF. We estimate the noise before irradiation for these layers as high as 1840e for the two-sensor modules. Figure 13 shows the S/N values for layer 2 and layer 3 again as a function of luminosity and for different temperatures. Generally, the S/N of the outer layers does not fall below 10, if they are kept at temperatures around T=0°C. The S/N performance loss in layer 2 can be reduced to less than 15%. For the other outer layers, an operation temperature of T=+5ºC seems to be sufficient.

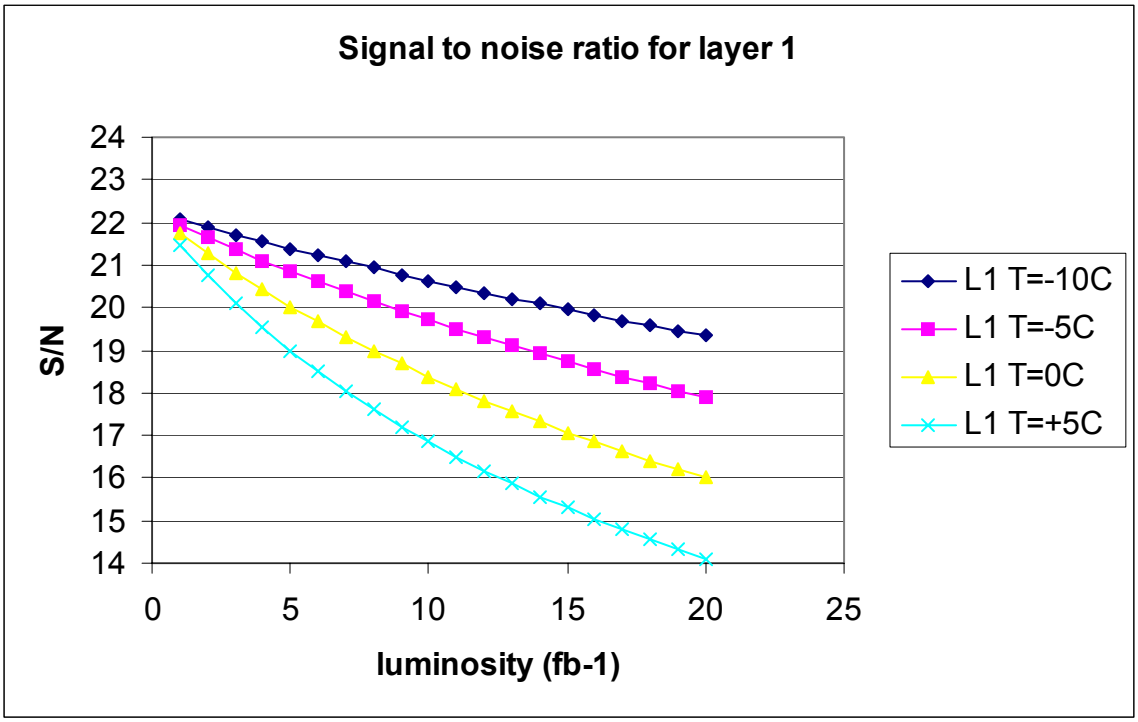


Figure 12: Signal to noise ratio for layer 1 as a function of luminosity for different running temperatures.

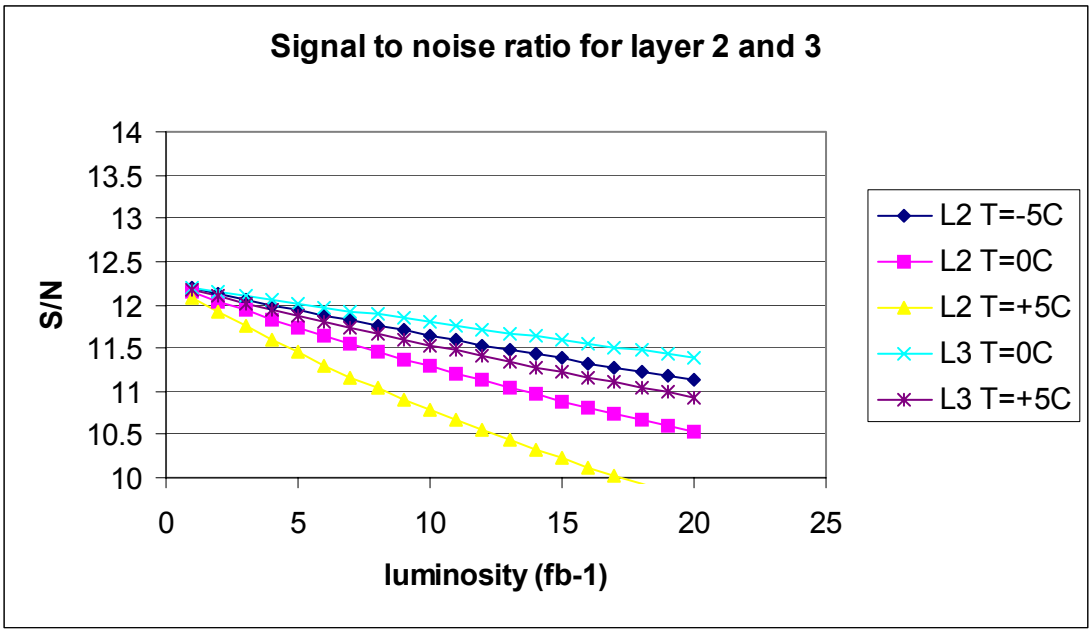


Figure 13. Signal to noise ratio for layer 2 and layer 3 at different temperatures.

In summary, based on our estimations of leakage currents, depletion voltage and S/N we intend to keep the silicon sensors (depending on the layer)at temperatures between T=–10°C and T=+5°C all times. The closer the silicon layer to the beam pipe is, the colder it should be operated.

The sensors of layer 3-5 can be kept between T=+5°C and T=0°C over the entire Run IIb since leakage current noise will not be the dominant noise source. Having the possibility to run layers 3-5 at T=0°C provides additional margin against higher radiation levels or current limitations in the HV supplies. In layer 2 the S/N performance degradation is below 15% if the sensors are maintained at 0°C. The S/N performance loss of 10% for layer 1 after $15fb^{-1}$ translates into an operating temperature of T=–5°C. The thermal profile of the FEA analysis suggests that such a low equivalent temperature for layer 1 can be reached by setting the coolant in the cooling circuit to –15°C. Finally, layer 0 has to be operated at T=–10°C. This low temperature limits shot noise and helps in suppressing the reverse annealing effects, especially if warm-up periods occur.

To check the breakdown behavior of the silicon sensors after irradiation and to compare our predictions to measured depletion voltage values, we have tested silicon sensors from several potential Run IIb vendors at the Radiation Damage Facility in the Fermilab Booster.

3.5 Radiation Testing of Silicon Sensors

3.5.1 Radiation Damage Facility

Radiation tests described here were carried out at the Radiation Damage Facility in the Fermilab Booster. The facility provides 8 GeV protons for various irradiation studies. The beam is ~0.5 cm in radius and is typically $>3x10^{11}$ protons per pulse, with a typical repetition rate of one pulse/3 sec. Beam flux is measured by a toroid and confirmed by irradiation of aluminum foils.

Detectors are mounted in a cold box, which maintains detector temperature at 5°C and allows for detector bias and monitoring. The box is in turn mounted on a x-y table which scans the detector assembly through the beam; insuring uniform irradiation.

Irradiation typically takes one shift. This intense irradiation can leave a substantial charge in the oxide and on detector surfaces. Detectors are then left at 5°C to "cool down" and anneal for ~1 week before testing.

3.5.2 Run IIa detector irradiation studies

To understand the expected lifetime of the Run IIa detector we performed a series of measurements with spare or grade B modules. These tests are described in detail in Ref. [17]. We used 3 different ladder/wedge types of double-sided detectors and one type of single sided detector. All detectors are processed on n-type bulk silicon material with a typical thickness of 300μm with integrated AC coupling and polysilicon bias resistors. The double-sided ladders had either 6, 9 or 14 readout chips on the their front end hybrid, which was directly glued on the silicon. The 6-chip detector is manufactured on a 6"-wafer technology and has 90° stereo strips on the n-side. The 9-chip detector is a stereo detector with a small angle view of 2°. The 14-chip module is a double-sided wedge-shaped detector with varying strip length and angle of ±15° on both sides.

The lifetime of the Run IIa detectors is likely to be determined by the limited voltage that can be applied across the AC coupling capacitors. These capacitors break down near 150 V and can only be safely operated to ~100 V. Thus, with split bias we expect to be limited to a total bias of 200 V. In addition during ladder testing we found that the Micron detectors are subject to microdischarge breakdown on the junction side. The breakdown voltage varies on a detector-to-detector basis but can limit the junction side bias to as low as 10 V. This effect switches sides upon type inversion and is partially mitigated on the n side by compensating effects of oxide charge.

In order to characterize the performance of the irradiated detectors and to understand their behavior after irradiation the following measurements have been carried out:

- leakage current measurements
- depletion voltage determination
- average noise determination
- number of noisy channels

Depletion voltage was measured by measuring the response to a 1064 nm laser, noise and current measurements were performed using our standard set of detector burn-in tests.

[17] J. Gardner et al. "Results from Irradiation Tests on DØ silicon Detectors at the Radiation Damage Facility at Fermilab", DØ Note in progress.

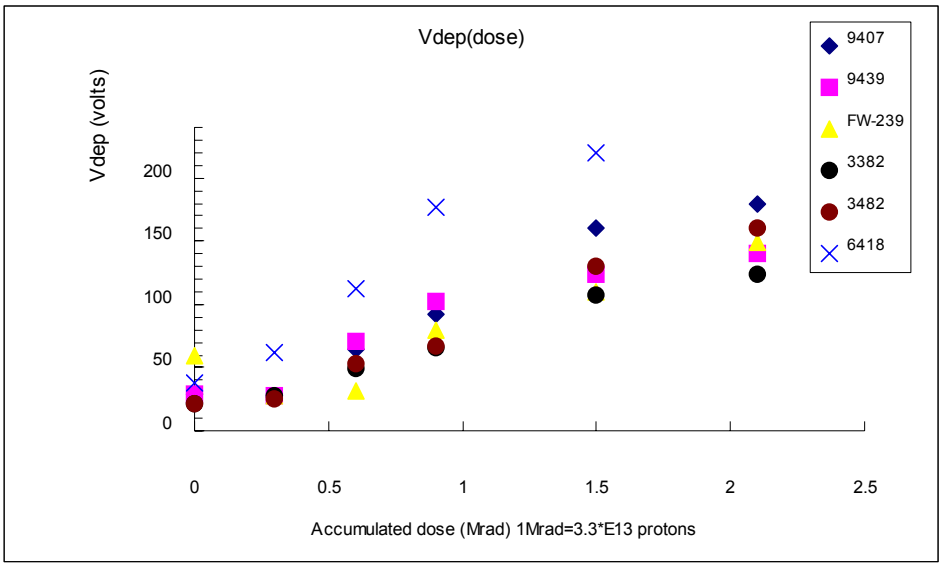


Figure 14. - Depletion voltage as a function of accumulated dose. Detector types 9xxx-layers 2,4; FWxxx-F wedge; 3xxx layers 1,3 barrels 1 and 6 (single sided); 6xxx – layers 1 and 3 barrels 2-5 (double sided double metal)

Figure 14 shows our results for depletion voltage and Table 8 gives the values. With the exception of the double sided double metal (DSDM) devices all detectors perform as expected. The DSDM detectors seem to have a depletion voltage at 1.5 MRad almost a factor of two higher than other devices. Since these detectors are at the inner radius of the silicon detector they will limit the lifetime of the tracker. The cause of this effect is not understood. All detectors were exposed at the same time and tested with identical setups. It is possible that the DSDM detectors are more susceptible to surface charge than simpler devices. We have performed additional irradiation studies with test structures to try to understand if this effect is due to bulk silicon properties or an effect of the fabrication. The tests indicate no problems with the bulk silicon.[18]

Table 8 Depletion Voltage measurements of detectors before and after irradiation.

N of the detector	Vd before irradiation	Vd after 2.1 MRad	Ratio
9407	29 ± 5	180 ± 30	6.2
9439	29 ± 5	140 ± 25	4.8
FW-239	59 ± 9	149 ± 25	2.5
3382	22 ± 4	124 ± 20	5.6
3482	22 ± 4	160 ± 25	7.3
6418	38 ± 6	Not found	

Figure 15 and Figure 16 show the noise in the ladders as a function of dose as measured in the burn-in test. The most probable pulse height for a MIP is ~26 ADC counts. The contribution

[18] S. Lager, Stockholm University Master's Thesis "Proton-Induced Radiation Damage in Double Sided Silicon Diodes and a General User Interface for the DØ Sequencer Low Voltage Power Supply.

from shot noise is ~0.8 ADC counts at 2.1 MRad. In general the noise rises from 1.5-2.0 counts to ~3 counts, giving a worst-case signal/noise ratio of 9:1. The DSDM detector (6418) has additional noise which rises to 5 counts on the n-side at 2.1 MRad. This is due to the onset of microdischarge on the n side of this ladder.

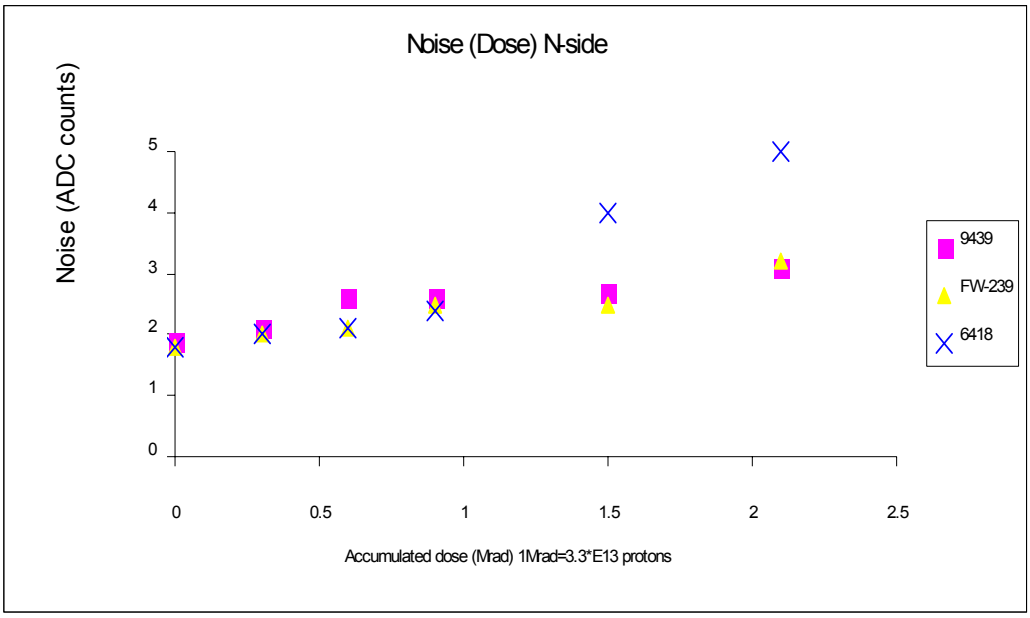


Figure 15 Noise in n-side of Run IIa ladders as a function of radiation dose.

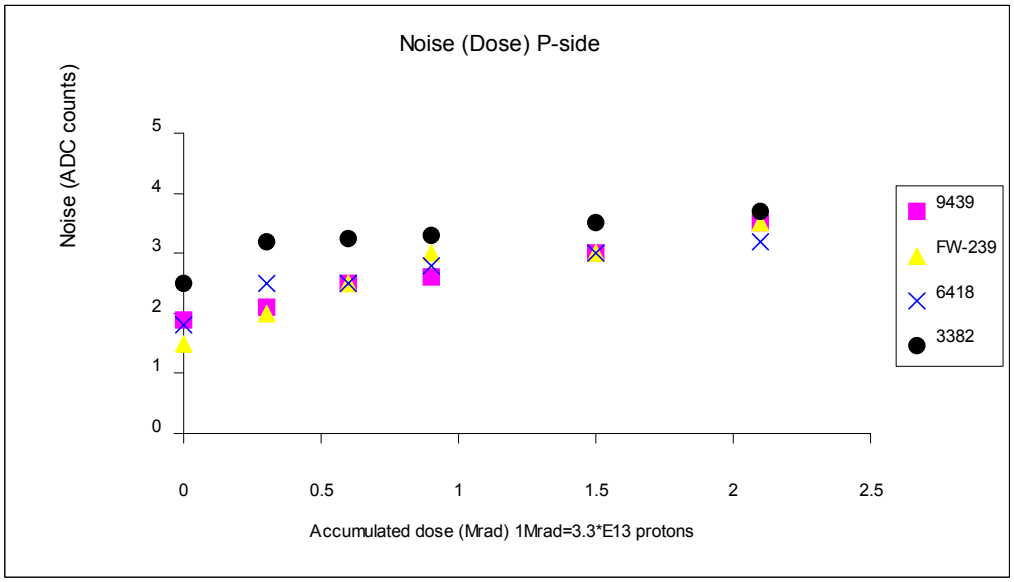


Figure 16. - Noise in p-side of Run IIa ladders as a function of radiation dose.

3.5.3 Run IIb detector irradiation studies

We have performed a set of irradiation studies on single sided detectors of the type to be used for Run IIb.[19] The detectors used were either CDF layer 00 devices (Hamamatsu, Micron, ST) or prototypes specifically for DØ (ELMA). Two Micron detectors were oxygenated, the ELMA devices were also oxygenated, but at a level too low to affect the depletion voltage. These detectors were exposed to 5, 10 and 15 MRad doses. We measured depletion voltage and leakage current after each exposure.

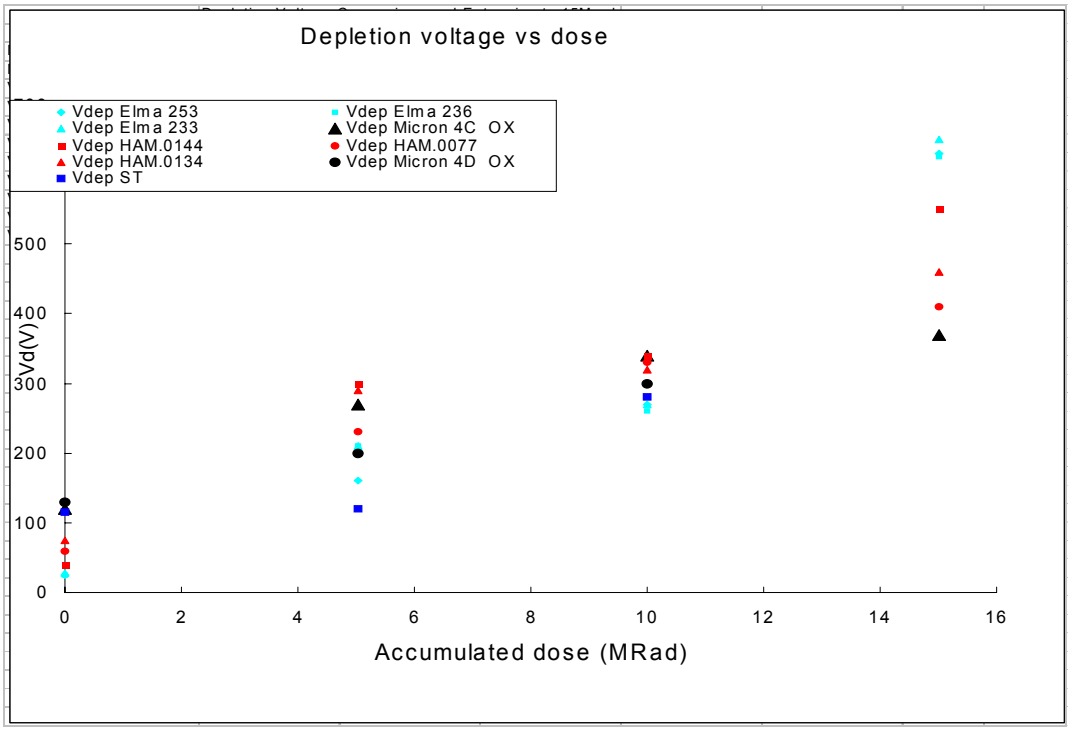


Figure 17. - Depletion voltage as a function of irradiation for Run IIb detectors.

Figure 17 shows the measured depletion voltage as a function of dose. The depletion voltage is estimated from the plateau of the detector response to a 1064 nm laser and has ~20% errors. The devices behave roughly as expected, although there is a considerable spread in the depletion voltage at 15 MRad. The ELMA detectors, which are fabricated using non-oxygenated silicon with a crystal orientation of <111>, have the worst behavior. The spread in depletion voltage is consistent with the variations among silicon types and manufacturers observed by LHC experiments.

[19] J. Gardner et al., "Studies on the Radiation Damage to Silicon Detectors for use in the DØ Run IIb Experiment", DØ Note 3958.

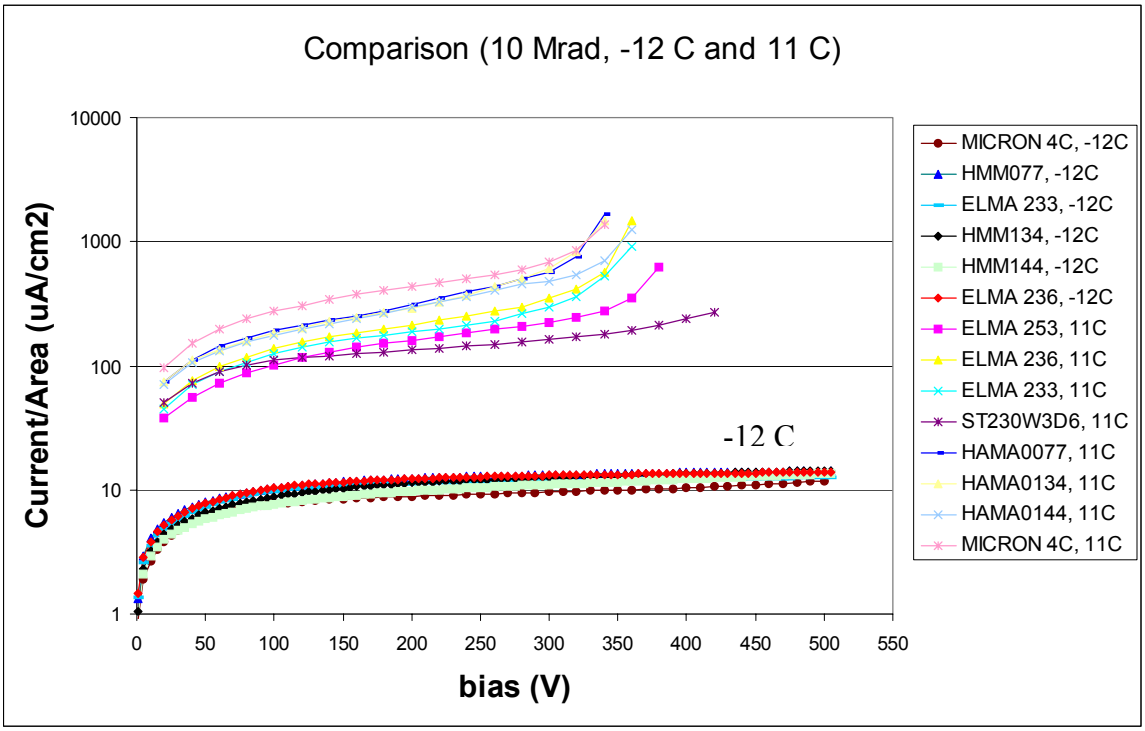


Figure 18 Leakage currents at +11 and –12 degrees C after 10 MRad

Leakage currents for all devices, presented in were found to be consistent with the usual $\alpha=3x10^{-17}$ A/cm^2 damage constant. The breakdown voltage depends on operating temperature as well as annealing time after the intense irradiation. None of the devices showed breakdown before full depletion under laser test conditions (near +10°C). Additional operating margin is available at our expected operating temperature of –10°C.

The results of these studies give us confidence that we can build a detector which can operate to 15 fb^{-1} and beyond. We plan to irradiate samples of prototype and production detectors to confirm their performance. We also expect to irradiate ladders bonded to SVX4 chips to measure ladder noise performance after irradiation.

3.6 Conclusion

The high integrated luminosity of Run IIb will necessarily result in a particularly harsh radiation environment. Reliable operation of silicon sensors in such conditions is crucial to the experiment's success. We were guided in our design and technology choice by our experience in Run IIa detector construction as well as by recent advancements in radiation hard silicon technology motivated primarily by the needs of LHC experiments. In Run IIb, DØ plans to use only single-sided single-metal silicon sensors, limiting them to only 3 types. Our estimates, supported by the results of the irradiation tests, show that these sensors will be able to withstand the radiation dose equivalent to more than 15 fb^{-1} with a significant safety margin in layers 0-5.

The depletion voltage for layer 0 sensors is expected to reach 300V for the assumed Tevatron Run IIb scenario of accumulating a luminosity of 13 fb^{-1} within 4 years. The layer 0 sensors will be specified to breakdown not earlier than 700V, providing enough flexibility in overbiasing these detectors. Warm periods of several weeks for maintenance should be carefully avoided in order to prevent reverse annealing. As an additional safety measure against the depletion voltage rise, the layer 0 sensors could be oxygenated. An oxygenation of these sensors is expected to slow down the depletion voltage growth after the type inversion. Further R&D studies are needed to confirm this approach.

4 MECHANICAL DESIGN, STRUCTURES, AND INFRASTRUCTURE

4.1 Overview

The mechanical design of the Run IIb silicon detector is challenging. It must satisfy strict requirements on material mass, on precision of construction and positioning, it must allow for signal readout and cooling of the detectors, and must satisfy overall size constraints imposed by the need to install the detector through the limited space between the calorimeter cryostats. In order to meet the latter requirement, the silicon for Run IIb will be divided about z = 0 into identical north and south barrel assemblies. That division addresses the limited installation space available after the end calorimeters have been opened 39" and allows a net length of silicon associated structures to exceed the 52" that would otherwise be available. Final connections between north and south assemblies will be made via reproducible ball mounts during installation at DØ. Testing and experience with the Run IIa silicon, which relied upon similar connections for support from the fiber tracker, demonstrated that a reproducibility of 2 μm is achieved with such ball mounts.

Each assembly comprises six silicon layers and is subdivided into an inner barrel with layers 0-1 and an outer barrel with layers 2-5. Inner and outer barrels will be fabricated individually, mated at SiDet to form either a north or a south barrel assembly, and brought to DØ as a completed, tested assembly. The inner diameter of those assemblies allows installation of a 1.16" outside diameter beryllium beam pipe through the silicon region after the barrel assemblies are in place at DØ. Figure 19 shows a plan view of the detector while Figure 20 shows an axial view.

In each of the north and south barrel assemblies, a double-walled cylinder, which is integral with the outer barrel, positions and supports a thin (~0.5 mm) carbon fiber reinforced resin (CFRR) silicon-positioning membrane near z = 0 and a thicker (~1 mm) CFRR outer silicon-positioning bulkhead at z = ±600 mm. A reproducible ball mount connection will be made between the support cylinder of the outer barrel and an additional cylinder extending from the outer positioning bulkhead to the end of fiber tracker barrel 1. The additional cylinder allows better access for precision CMM measurements of silicon positions and better access for work on the ends of silicon sub-assemblies. After all assemblies are in place and all mechanical connections are completed, the equivalent of a single 356 mm outside diameter support cylinder will extend ~1650 mm from one end of fiber tracker barrel 1 to the other.

Silicon sensors of the inner barrel, layers 0 and 1, are mounted on facets of quasi-polygonal cylindrical structures similar to the one used in Run IIa for CDF layer 00. All inner barrel sensors will be placed so that their traces are axial. The inner barrel is supported by the silicon-positioning membrane and by the silicon-positioning bulkhead of the outer barrel. Silicon of the outer barrel, layers 2-5, is contained in 84 staves, which are supported from the silicon-positioning membrane and the outer silicon-positioning bulkhead of the barrel. In order to provide azimuthal overlap between sensors, each silicon layer will be divided into inner and outer sub-layers "a" and "b". Each of the staves of the outer barrel will contain a set of sensors

oriented so that their traces are axial and a set of sensors oriented to provide small angle stereo information. Table 9 gives the radii, lengths, and number of phi segments for the detector.

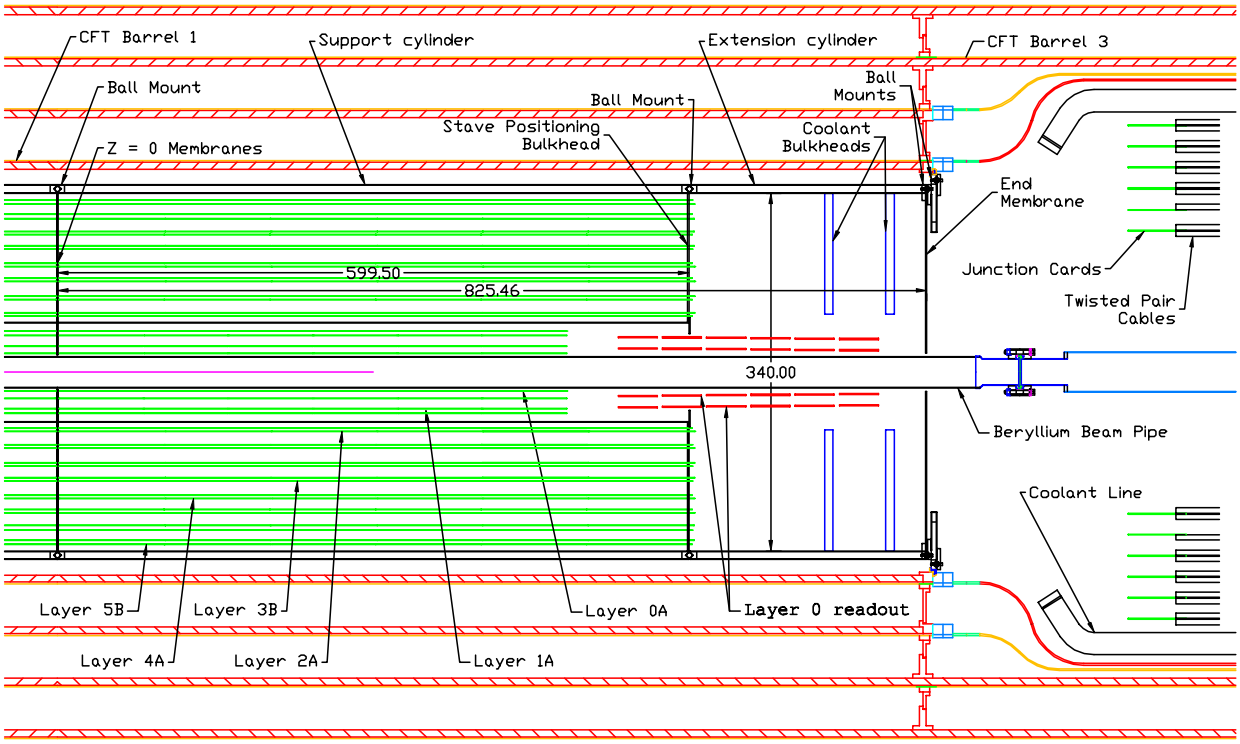


Figure 19 - Plan view of the silicon tracker within the fiber tracker (all lengths in mm). The silicon tracker is divided into north and south assemblies about z = 0. For each of the assemblies, layers 0-1 and layers 2-5 are fabricated as separate mechanical structures and mated at SiDet. To facilitate CMM measurements, only the portion of the support cylinder from z = 0 to z = 600 mm will be present during layer 2-5 stave installation and mating with layers 0-1. Coolant distribution bulkheads, coolant connecting tubing, and extension cylinders will be added when that work is complete. The lengths of the north and south assemblies match those of the Run IIa central silicon and utilize the Run IIa mounts on the ends of the fiber tracker. North and south assemblies will be joined during installation at DØ to form a full-length structure designed for support only at its ends Lengths of layers have been chosen to provide good acceptance for high p_T physics taking into account the expected length of the luminous region. The silicon of layers 2-5 is shown at the central radii of sensors. CFRR, hybrid, and cooling structures of staves are not shown. In all staves, those structures extend to the z = 600 mm positioning bulkhead.

Table 9 - Silicon geometric parameters of a barrel assembly (units = mm)

Layer	0a	0b	1a	1b	2a	2b	3a	3b	4a	4b	5a	5b
R axial	18.0	24.8	34.8	39.0	54.6	70.0	89.5	103.7	116.5	130.5	148.8	162.7
R stereo	---	---	---	---	57.4	72.9	86.6	100.8	119.4	133.4	146.0	159.9
Length(z)	475	475	479	479	601	601	601	601	601	601	601	601
# Phi	6	6	6	6	6	6	9	9	12	12	15	15

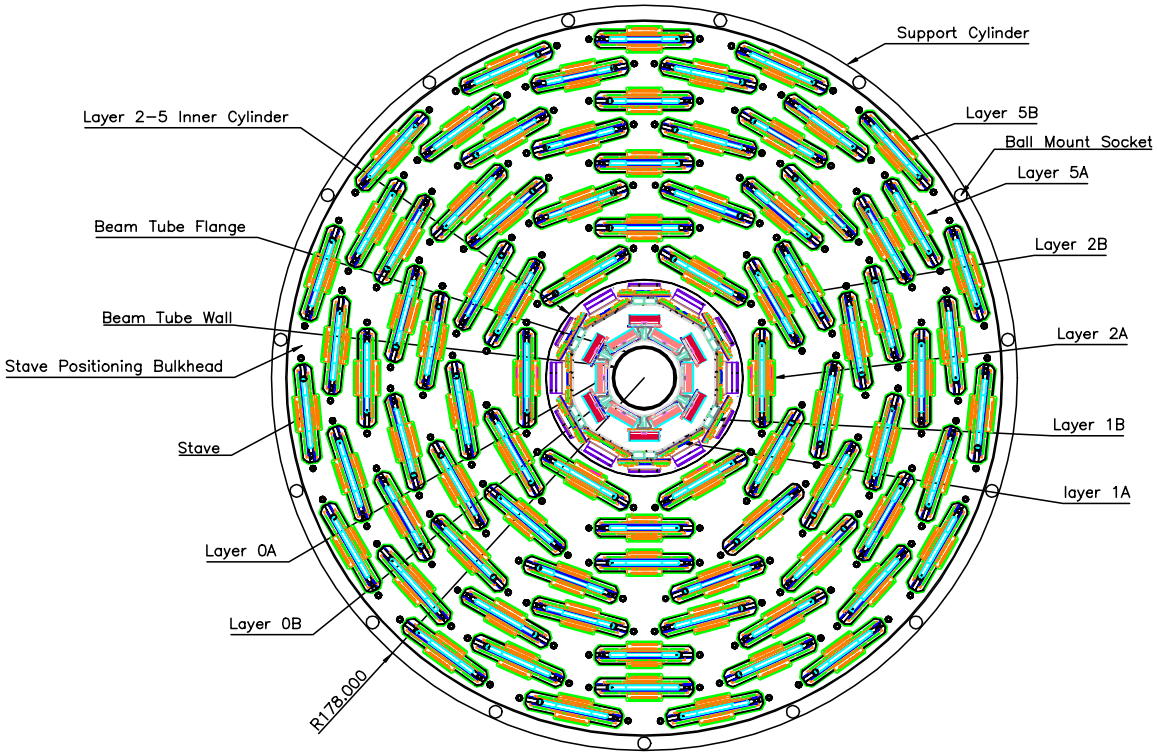


Figure 20 - End view of the layer 0-1 module, layer 2-5 staves and the outer silicon-positioning bulkhead. Silicon radii and sensor widths have been chosen to provide >99% r-phi geometric acceptance for tracks of p_T > 1.5 GeV/c originating within 2 mm of the nominal beamline. The design of the layer 0-1 and layer 2-5 assemblies allows removal of layers 0-1 at DØ and replacement with good precision. The inner diameter of layer 0 has been chosen to permit beam pipe installation after all silicon is in place at DØ.

4.2 Overall Support Structure

The main structural components must provide accurate, stable positioning of both the inner and outer detector elements. The main components are a double-walled carbon fiber cylinder that resides outside the outermost silicon layer and a set of bulkheads that provide the precision mounting points for the outer layer staves and the inner layer sub-assemblies. The details of these components and the alignment constraints are provided in the following sub-sections.

4.2.1 Outer support cylinders, stave positioning bulkheads, and z = 0 membranes

The design of the 356 mm outside diameter support cylinders is based upon that of the 306 mm outside diameter cylinders of Run IIa. Each cylinder will have inner and outer carbon fiber reinforced resin (CFRR) walls ~0.56 mm thick separated by CFRR "ribs" ~0.40 mm thick. Seven or more layers of flame retardant free, high modulus (>90 Msi), unidirectional fiber prepreg will be used for the shells and six or more layers for the ribs. The number of layers will depend upon the thickness of the high modulus material which is available. Individual CFRR pieces are cured at elevated temperature and then bonded to one another at room temperature with epoxy. Based upon the performance of the Run IIa cylinders, beam deflection should be less than 40 μm over a length of 1650 mm. Compensation for that deflection can be made by offsetting either the z = 0 positioning membranes or the outer positioning bulkheads when they are glued to the cylinder. The ribs, end rings, membranes, and bulkheads stiffen the completed structure against out-of-round distortions. Based upon performance of Run IIa cylinders before openings were cut for silicon installation, out-of-round distortions should be minimal. However, prototypes will need to be fabricated and measured to verify beam and out-of-round deflections.

The CFRR stave-positioning bulkhead will be made of multiple layers of flame-retardant-free, high modulus (>90 Msi), unidirectional fiber prepreg with an elevated temperature cure. These bulkheads are expected to be a sandwich structure of two ~0.5mm thick CFRR panels with ruby bearings mounted to the inside face of the outer panel. The sandwich structure provides stiffness to resist longitudinal loads from the staves, particularly coming from the stave electrical and cooling services. Openings in the bulkheads are intended to match stave profiles, including cables, and to provide 0.5 mm clearance about the full stave periphery. Staves will be installed through the openings and located by pins which engage locating bearings glued into the bulkhead. We plan to locate the bearings using high-precision fixturing as they are glued into place. The intent is to place the stave locating bearings and the stave pins which engage them well enough to allow interchangeability among staves.

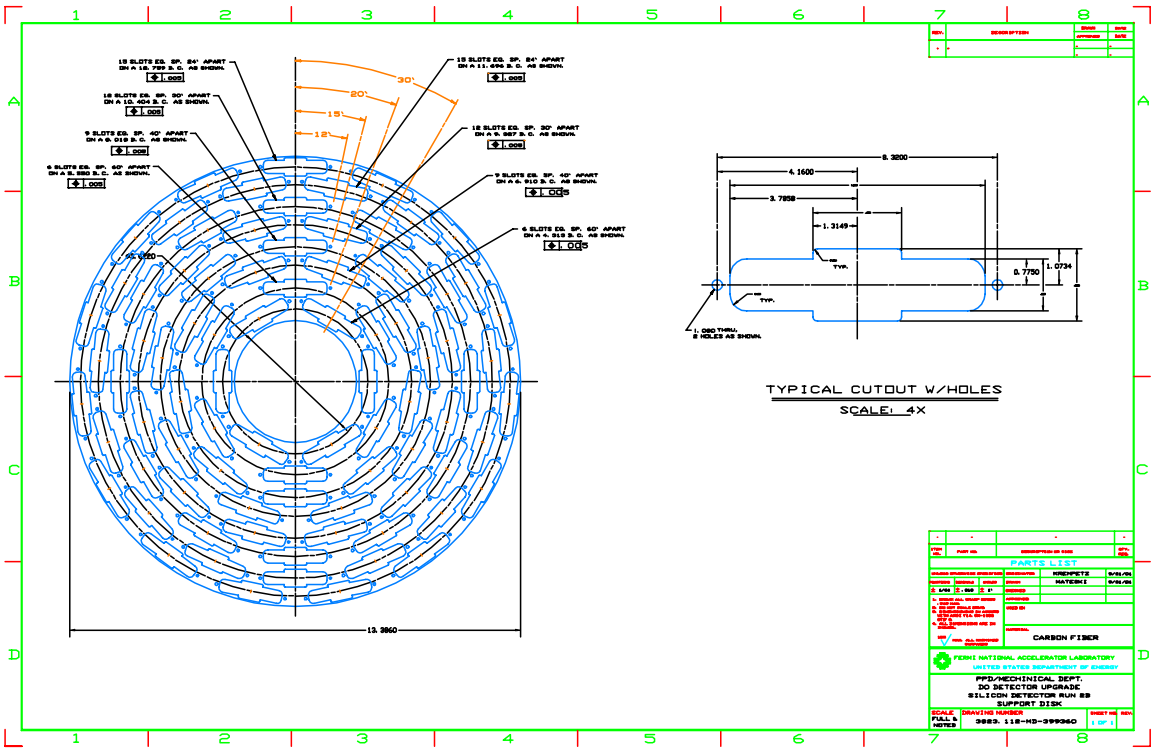


Figure 21 - Cut profile supplied to Lab 8 for a prototype positioning bulkhead. The profile of a stave opening is shown on the right; the locations of openings are shown on the left.

The CFRR z = 0 membrane will be made in a similar manner as the z=600mm bulkheads. Again, a sandwich structure will be used, but in this case the innermost panel could be a full disk with an opening for the beam pipe, since staves do not pass through it. In practice, openings will be cut in the membrane to reduce material. A design for the openings remains to be developed. Bearings will be glued onto the outer face of the innermost membrane to engage stave-positioning pins. Local reinforcement will be provided at each bearing location. A precision fixture will be used to position bearings as they are glued into place.

CFRR end rings for each cylinder include sockets of the ball mounts and features to allow one cylinder to be securely coupled to the next. Based upon Run IIa experience, twelve ball mounts, evenly space in azimuth, should be sufficient per end ring. Due to the 30-fold symmetry of the outer silicon layer we anticipate using 15 ball mounts. Screws or studs through the balls will be used to couple cylinders. Openings through the outer walls of cylinders, with suitable reinforcement, will provide access to install and tighten fasteners. The end rings will be made of multiple layers of flame retardant free, high modulus (>90 Msi), unidirectional fiber prepreg with an elevated temperature cure. Precision jig plates will be used to position the ball mount openings.

A CMM will be needed as pieces of cylinder assemblies are glued to one another in order to establish clockings and offsets. Whenever practical, end rings will be mated during the gluing process. A full procedure for establishing end ring clockings and offsets remains to be developed. In general, we plan to employ ruby or sapphire balls as reference features for CMM touch probe measurements. Positions of stave locating features can be measured in a coordinate system established by these reference features.

4.2.2 Alignment precision and survey accuracy

All alignment constants, both at the trigger level and offline, assume that the silicon sensors are perfect planes. Six constants are used, three offsets used to define the position of the center of the sensor and three Euler angles used to define the rotations of the sensor about that center. Survey data taken during assembly, or obtained from offline alignment with tracks, can be used to determine the alignment constants for the tracker. No real-time alignment constants are available so it is critical for the trigger that the detector be stable over time scales of weeks to months.

It is important to make a clear distinction between the precision required for the placement of the sensors and the required survey accuracy. The physical alignment precision for the sensors is determined primarily by the requirements of the impact parameter trigger, which is used to identify events with tracks originating from the decay of heavy quarks outside the beam spot. Having satisfied these constraints, other considerations, such as having tractable offline alignment constants, are also satisfied. The survey accuracy, whether done using optical or mechanical survey on the bench, or using tracks *in situ*, should have accuracy on the scale of the intrinsic device resolution (≈8μ transverse to the sensor strips).

No stereo information is available at the trigger level so the trigger is most sensitive to rotations about the two axes transverse to the beam line (pitch and yaw) that result in Z-dependent r-ϕ errors. Deviations from planarity are also important, both at the trigger level and for the offline analyses since these are not corrected for. The figure of merit for location of sensors is that, relative to the beam spot size, the errors introduced have a small effect on the impact parameter resolution. For a rotation about an axis perpendicular to the plane of the sensors (yaw), the desired alignment tolerance is <10μ over the length of a readout segment. The pitch angle affects strips at the edges of the sensors, but not at the center. For a radial deviation dR at an angle ϕ from the center of the sensor, the transverse measurement error dX is given by $dX=dR\tan\phi$. Local radial displacements due to a lack of sensor flatness contribute in the same way as an overall pitch of the sensor. Again, the desired tolerance is dX<10μ within a readout segment.

4.3 Layer 0-1 Silicon Mechanical Support Structure

4.3.1 Introduction

The Layer 0 and 1 silicon support structures described in this TDR are carbon fiber structures with each layer consisting of an inner and outer carbon fiber shell. In L1 a pyrolytic graphite layer that transfers heat to the cooling tubes is inserted between the inner and outer layers. Our design is geometrically similar to the Run IIa CDF inner silicon support structure that is also made from carbon fiber composite. In L0 the hybrids are cooled by a separate system that is designed in two layers to facilitate installation of the hybrids and the associated cables. We have chosen carbon fiber cooling tubes with relatively high axial thermal conductivity in order to meet our cooling requirements. The manifolds needed to combine all of the cooling circuits in one inlet and one outlet connection also serve as structural bulkheads. A third bulkhead provides the

support point for connecting L0 to the inside of L1 and L1 to the L2-L5 structure. The other support point at Z=0 consists of a set of discs and precision pins.

We have developed a full solid CAD model of the design that includes all components and cables. We have a complete mechanical and thermal FEA analysis for Layer 1 that is described herein. We measured the basic tensile and thermal properties of the carbon fiber materials we are using and experimentally verified that we can use lay-up theory to obtain tensile and thermal properties for the specific structures we are using, see section 4.3.4.

A brief description of the work done to date on fabrication techniques and how we obtain mechanical precision is given in section 4.3.5.

4.3.2 Design of the Layer 0-1 Silicon Mechanical Support Structure

The silicon sensors and associated electronics in layer 0 and layer 1 require a very lightweight and rigid support structure, constructed to very demanding mechanical tolerances. Provision must also be made for cooling of the sensors and the hybrid electronics. Carbon fiber composite provides the most effective combination of low density and rigidity along with manufacturing flexibility. A research study was made to determine the most effective fiber type and lay-up and to examine the manufacturing issues involved. The most effective combination was found to be a K13C2U high modulus, high thermal conductivity fiber. This is used in a 6-layer $[0^o/20^o/-20^o]_s$ lay-up in the castellated shells and in a 4-layer $[0^o/90^o]_s$ lay-up for the inner tube. The cooling tubes use K1392U fiber in a 4-layer $[25^o/-25^o]_s$lay-up. This was needed to permit lay-up around the small tube radii. Both composite materials use a cyanate ester resin that has high radiation tolerance and very low moisture absorption. To meet the grounding requirements specified by the Electronics Group, a layer of thin aluminum foil is incorporated in the layup as needed.

4.3.2.1 L0 Structure

The L0 layer of the detector is shown in Figure 22. The support structure (Figure 23) consists of a backbone tube and an outer, castellated tube on which the sensors are mounted. This structure extends from Z=0 to Z=480 mm. The hybrids are mounted separately from the sensors on structures, shown in Figure 24, that extend out to Z=806 mm. To provide further bending stiffness, the inner carbon fiber tube has its wall thickness doubled in the region of the hybrids.

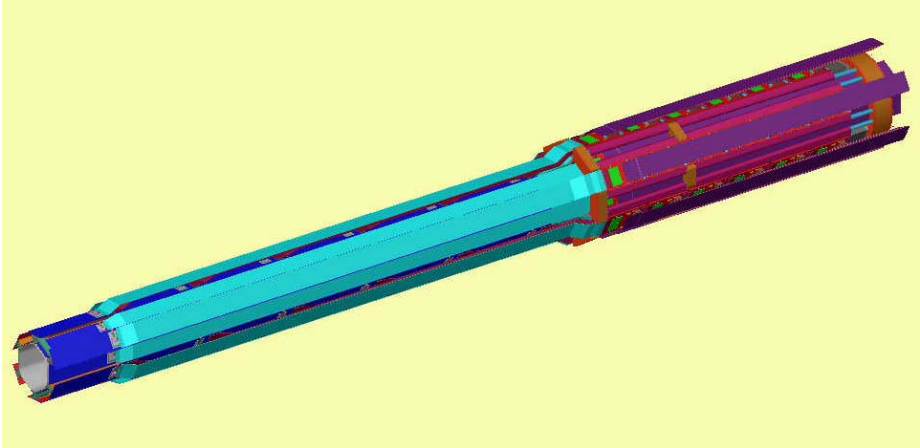


Figure 22: Complete layer 0 assembly.

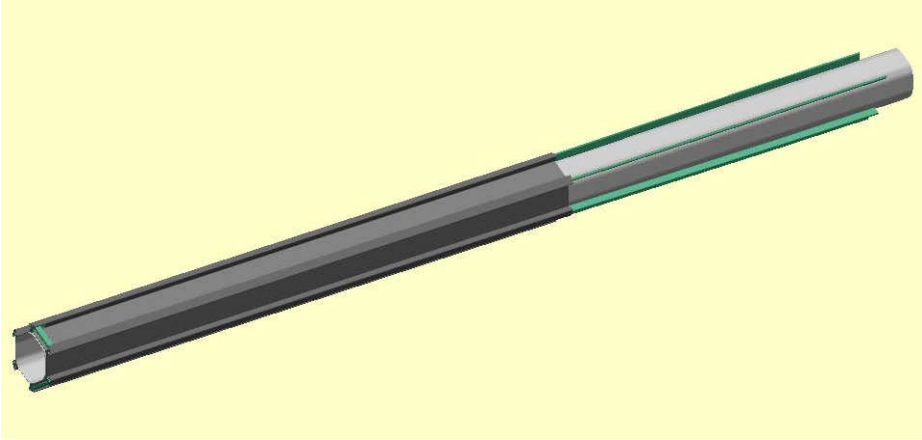


Figure 23: Layer 0 support structure.

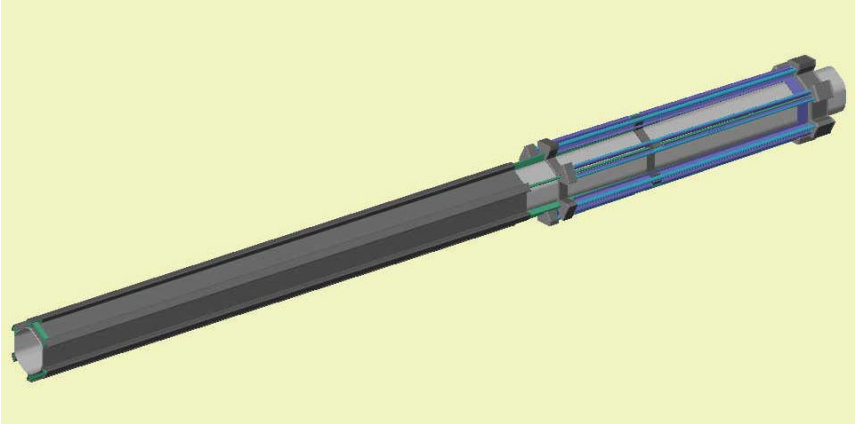


Figure 24: Hybrid support structure (A layer only is shown).

The silicon sensors are mounted on the castellated tube using epoxy adhesive. Two insulating layers of Kapton separate the silicon backplane, operating at up to 700V, from the grounded carbon/epoxy structure.

Note that there are two layers of these sensors at different radii (layers 0a and 0b). Analog cables connect each sensor to its specific hybrid. A carbon fiber cooling tube is embedded in the castellation below each of the outer silicon sensors as shown in Figure 25. A water/40% glycol mixture circulates through these tubes to maintain the desired chip temperature. The flow is turned around at Z=0 as shown in Figure 26.

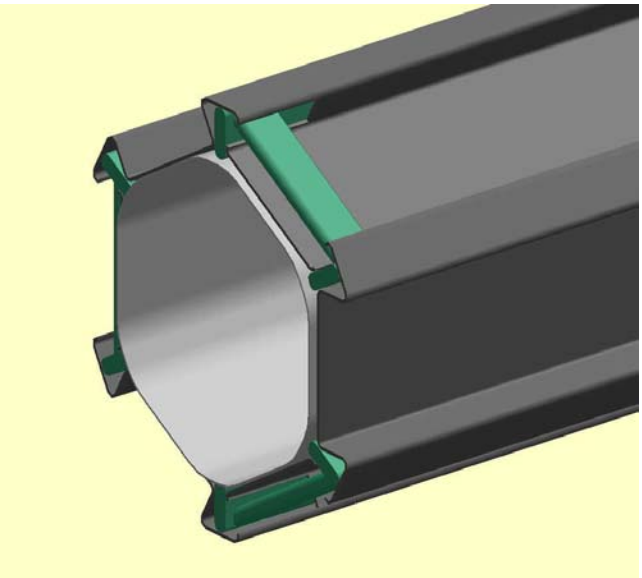


Figure 25: Cooling tubes for the sensors are inside the castellations.

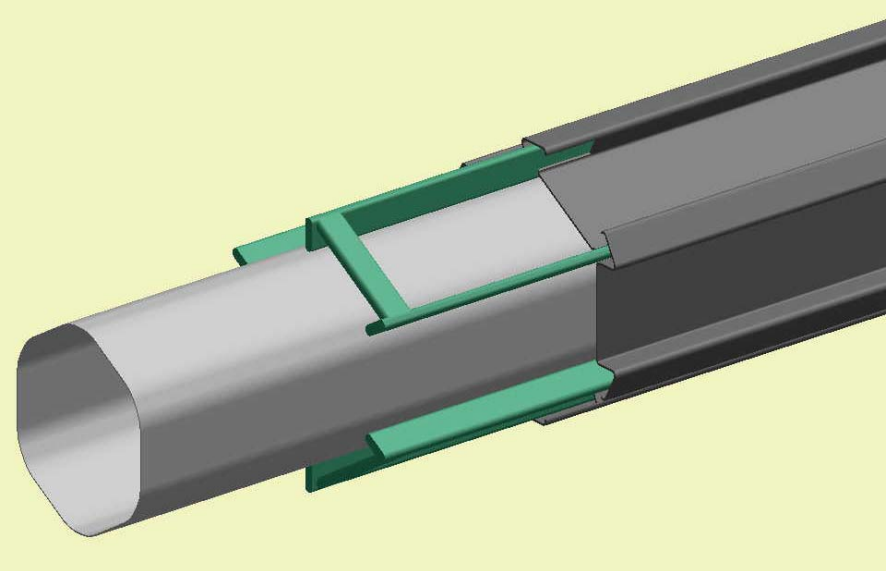


Figure 26: Exploded view of cooling tubes showing the turnaround pipe.

The hybrids have a separate cooling system. This consists of two rings of hybrid supports and cooling tubes. Each ring consists of six sets of hybrid support rails and cooling tubes connected by three bulkheads. These rings are pre-assembled and checked for coolant leaks. The inner (L0a) ring is shown in Figure 27.

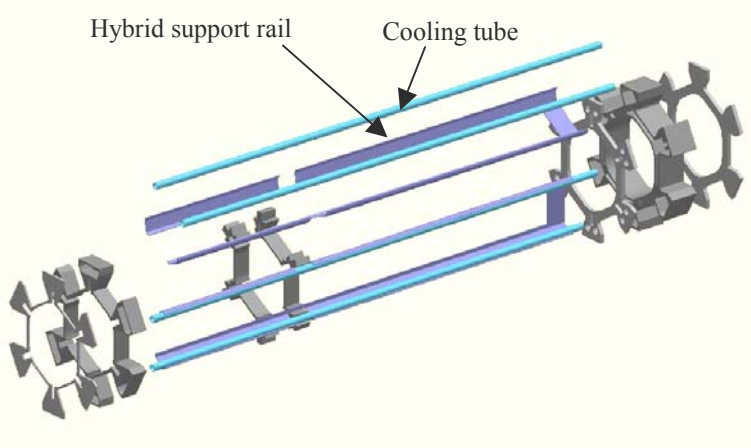


Figure 27: Exploded view of the support and cooling structure for the L0a hybrids. Only a few of the cooling tubes are shown for clarity.

The innermost bulkhead provides a turnaround path for the sets of cooling tubes. The outer surface is sealed by simple caps as shown (Figure 28).

The outer bulkhead (Figure 29) acts as a cooling manifold to collect the flow from the six lines cooling the hybrids and the flow from the six lines cooling the silicon sensors. This manifold/bulkhead is divided into two isolated annular compartments. One of these connects to the inlet coolant supply line and feeds fluid to the cooling systems. The other collects the coolant outflow and connects to the system coolant outlet line. The supply lines to the silicon sensors are isolated from the hybrid heat load allowing for delivery of the coldest possible fluid to the sensor region.

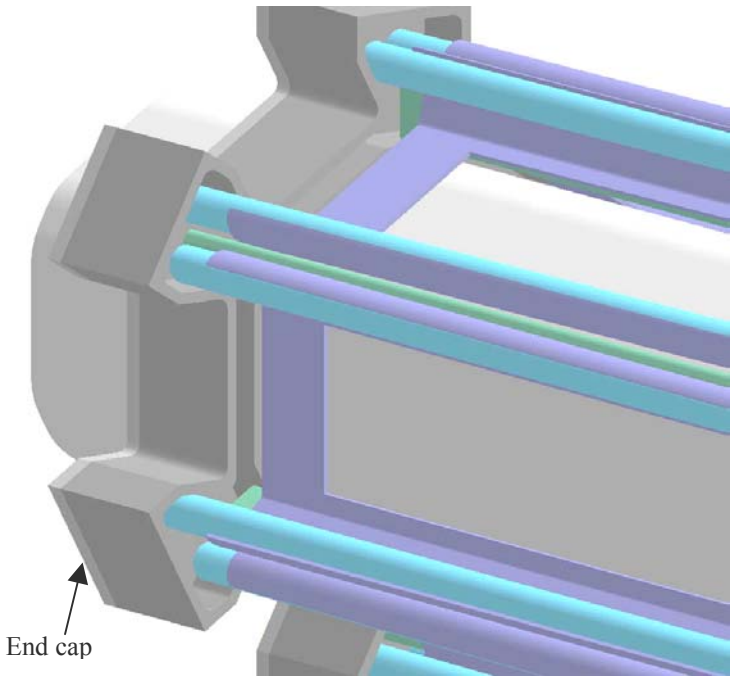


Figure 28: Inner bulkhead of L0a hybrid cooling structure.

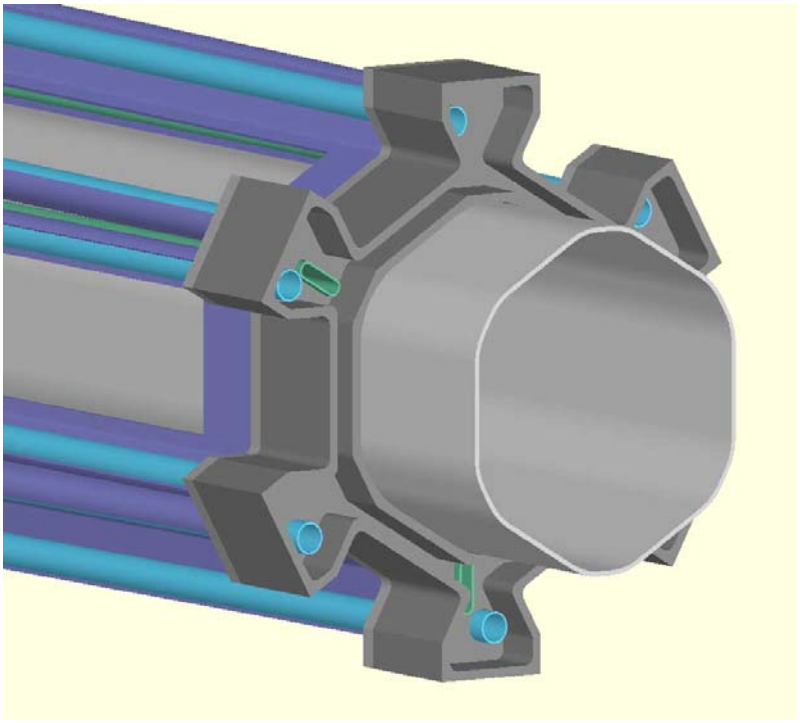


Figure 29: Outer bulkhead showing one of the cooling manifolds exposed.

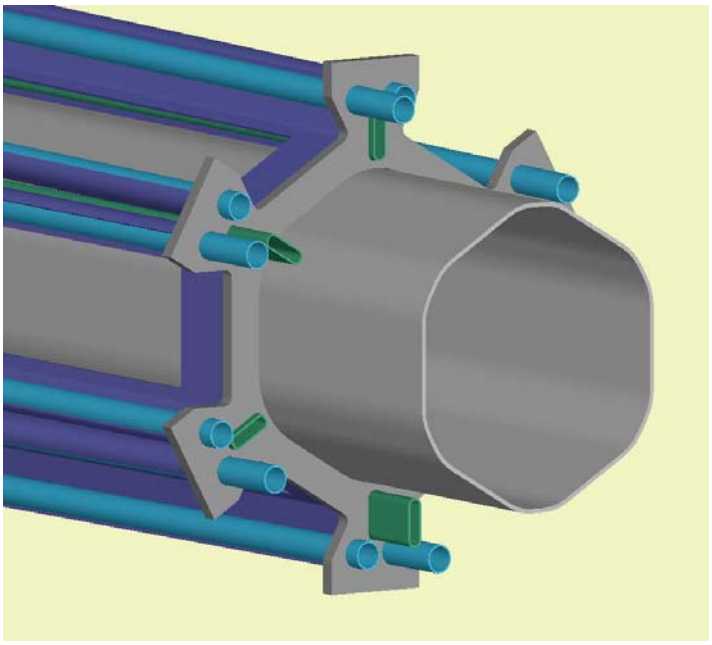


Figure 30: Cooling tubes end in the manifolds of the outer bulkhead.

The inner (L0a) ring is installed on the extension of the inner carbon fiber tube and the L0a layer sensors and hybrids are then installed and tested. The outer (L0b) ring (Figure 31) has a similar structure and has similar bulkhead/manifolds (Figure 32). It is installed over the L0a ring (Figure 33) and the remaining sensors and hybrids are installed.

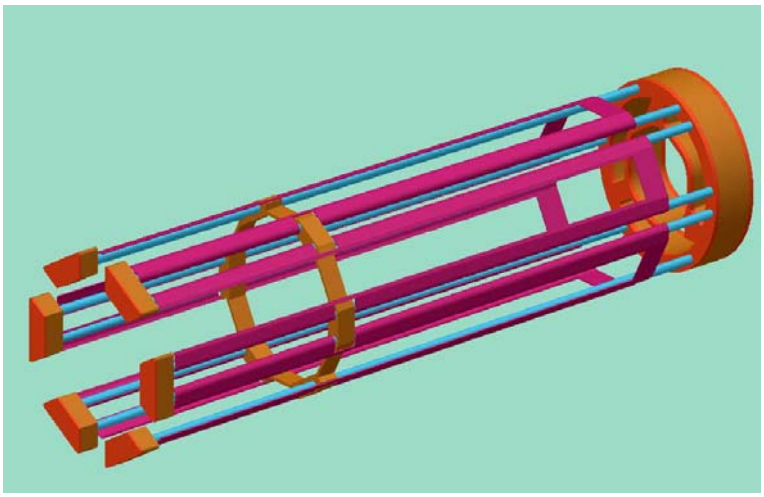


Figure 31: Support and cooling structure for the L0b hybrids.

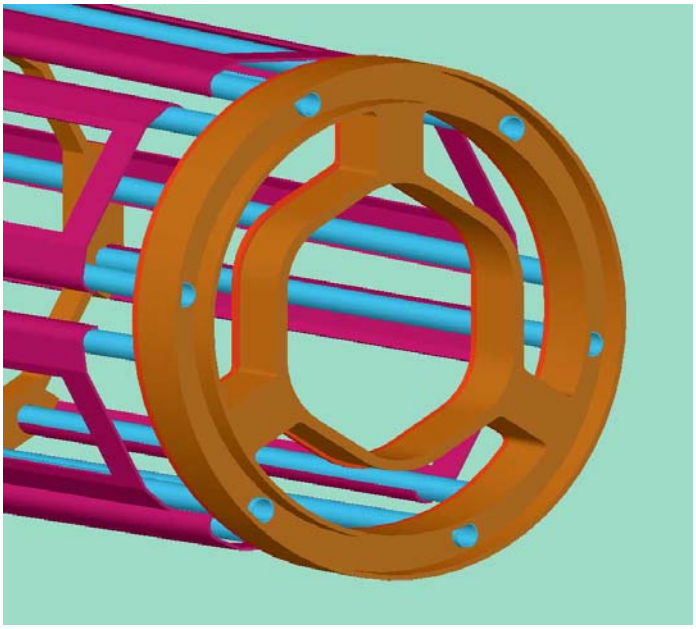


Figure 32: Outer bulkhead for the L0b hybrid support structure.

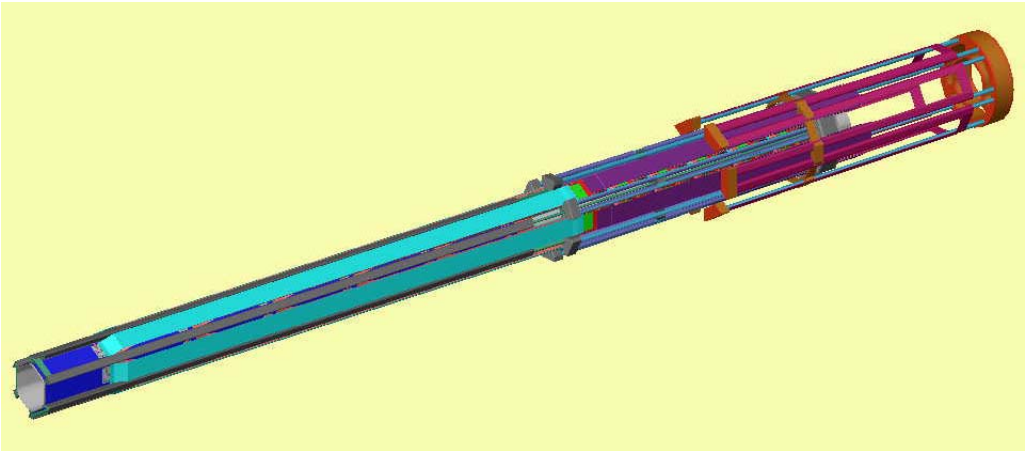


Figure 33: Installation of theL0b -layer cooling structure over the completed layer A.

4.3.2.2 L1 Structure

The L1 layer of the silicon detector is shown in Figure 34. This is very similar to L0. The major difference is that the hybrid circuits are mounted on and connected to the silicon sensors directly without the use of analog cables. Digital cables connect hybrids to the outside world.

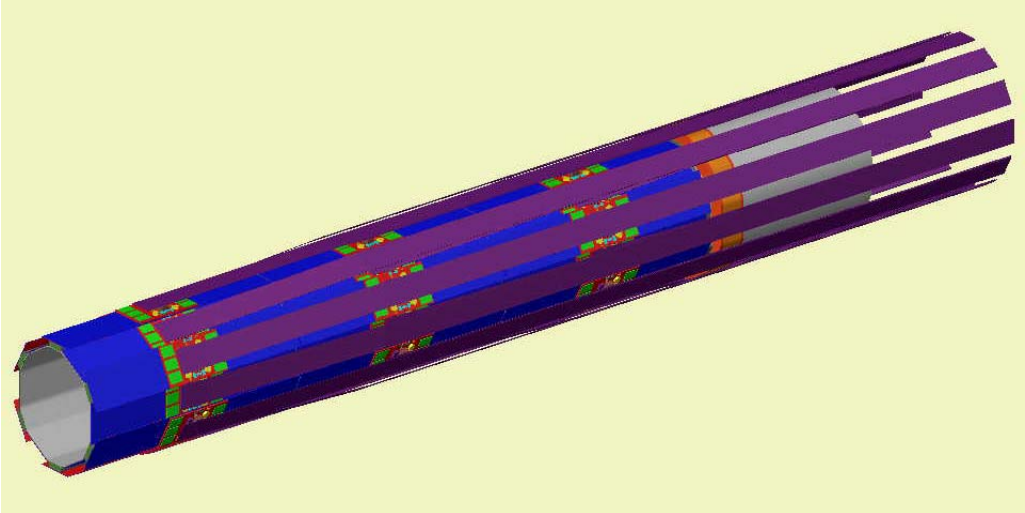


Figure 34: Complete L1 assembly.

The sensor/hybrid modules are mounted on a structure consisting of a castellated carbon fiber shell and an inner carbon fiber tube as shown in Figure 35. Two carbon fiber cooling tubes are embedded in each castellation (Figure 36). A layer of pyrolytic graphite is incorporated in the structure to provide a better thermal conduction path. Two layers of Kapton isolate the sensor backplanes, designed to operate at up to 700V, from the grounded conductive carbon fiber and graphite layers.

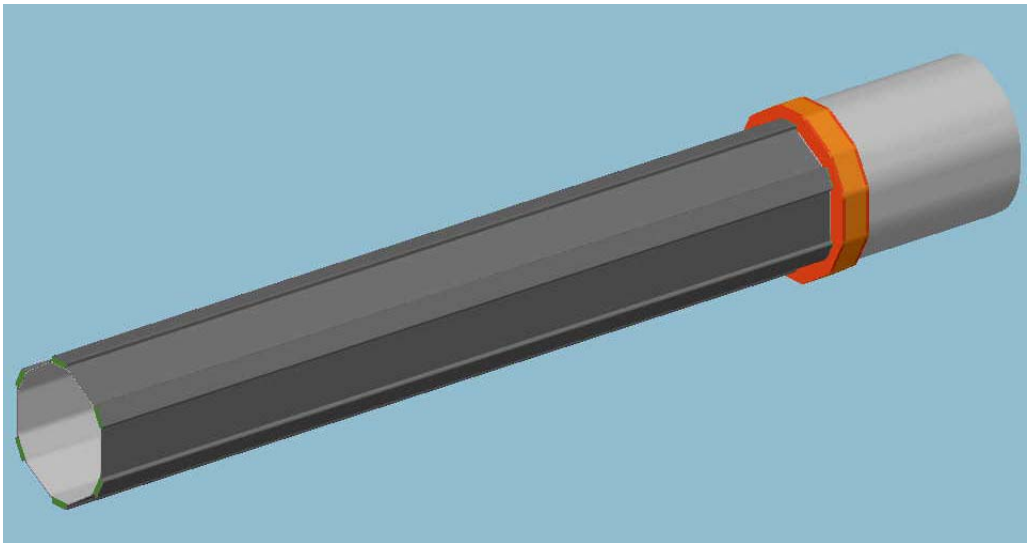


Figure 35: Support structure for L1.

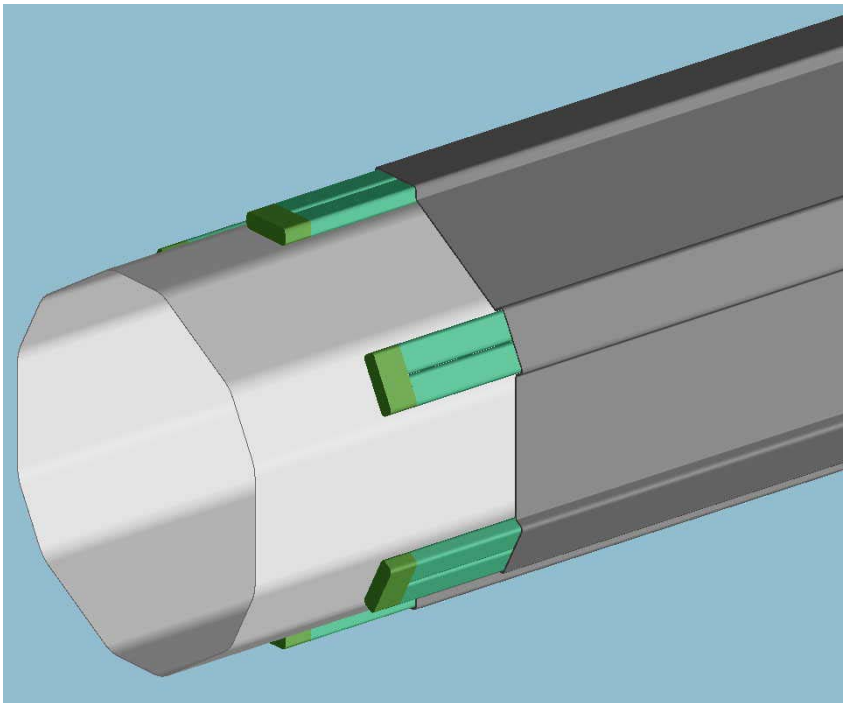


Figure 36: Exploded view showing the cooling tubes in the castellation and the turnaround.

The tubes in the castellations are turned around at Z=0. At the other end, these tubes end in a cooling manifold/bulkhead that uses the same design as that used in L0. This bulkhead also acts as a structural element (Figure 37 and Figure 38) to connect the sensor/hybrid support to a carbon fiber extension tube needed to provide support points for the L0-L1 connection and the overall support to the L2-L5 structure.

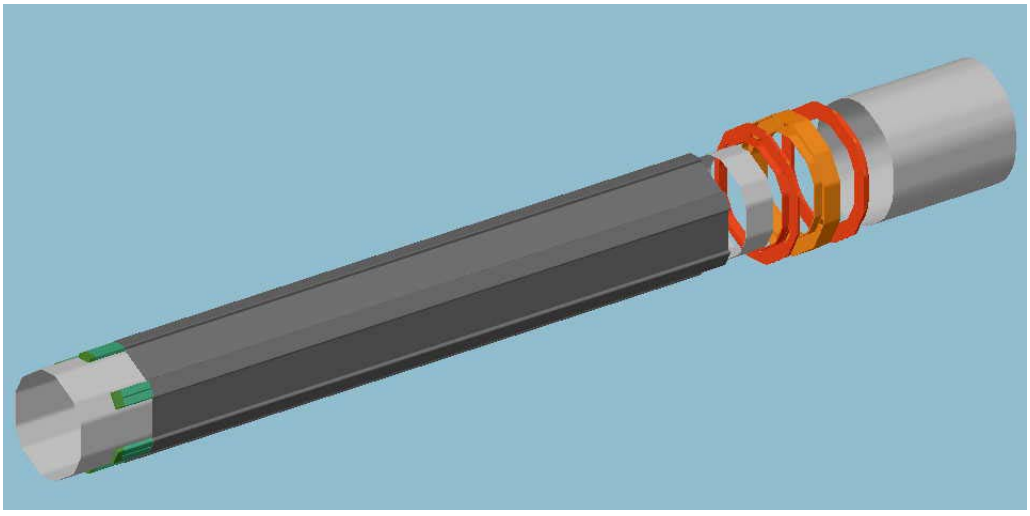


Figure 37: L1 support structure. The bulkhead/manifold also acts as a structural element.

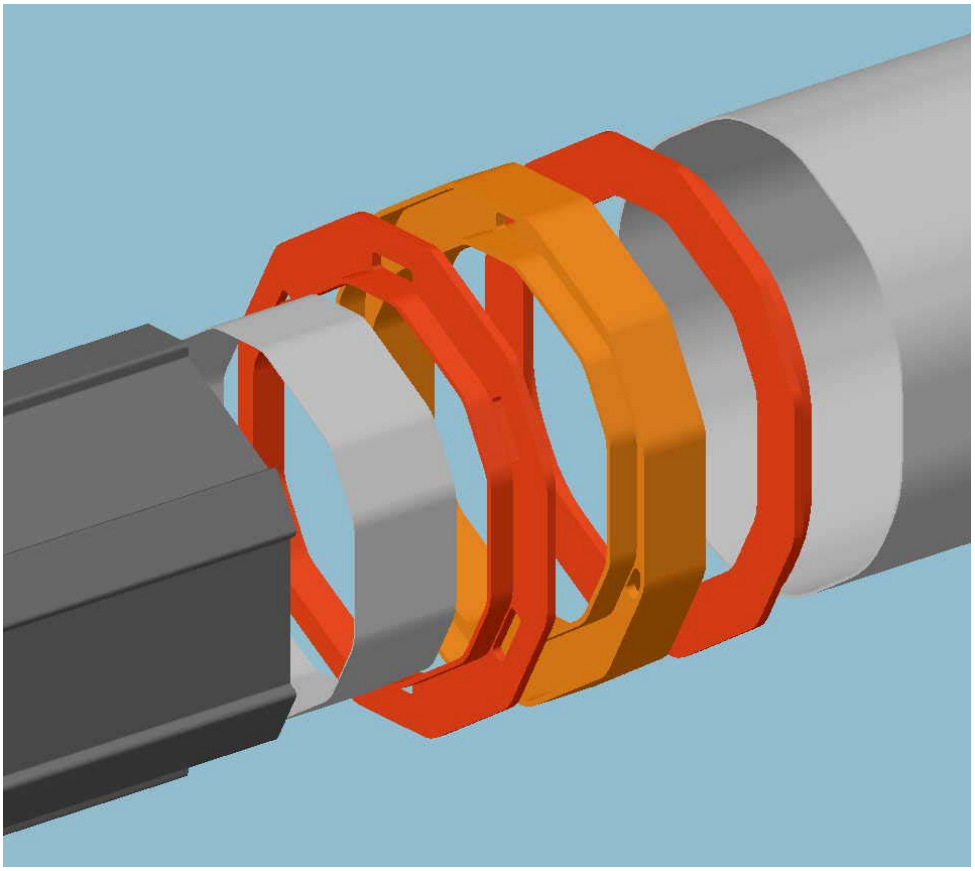


Figure 38: Exploded view showing details of the coolant bulkhead/manifold.

4.3.2.3 L0/L1 Assembly

The L0 and L1 mechanical structures have to be assembled into a single structure after the silicon, hybrids and cables have been attached. At Z=0 this is accomplished by simple disk shaped membranes (Figure 39).

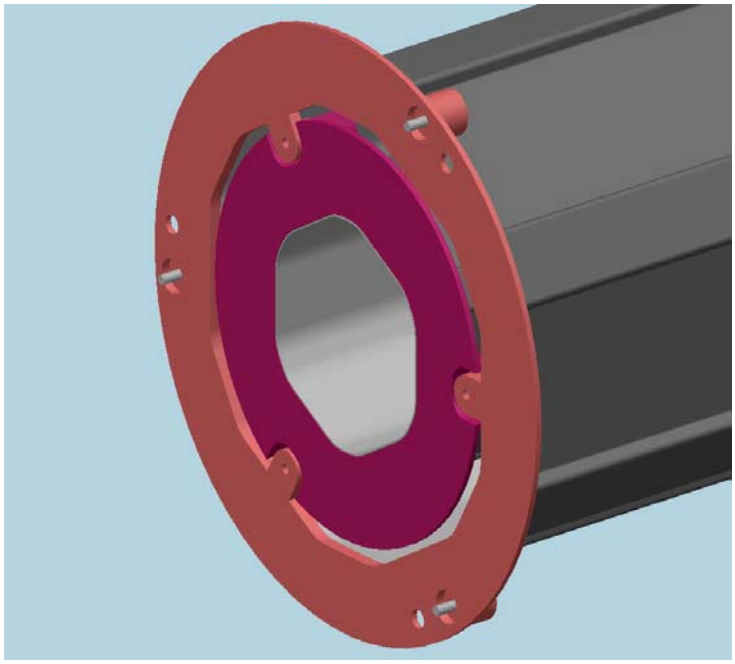


Figure 39: Support membranes at Z=0 connects L0 to L1 and L1 to L2-5.

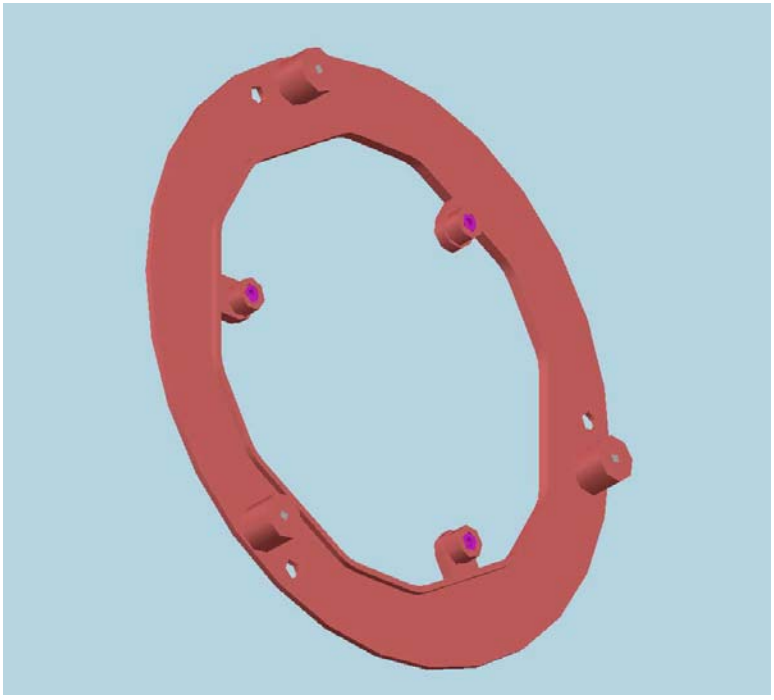


Figure 40: L1 to L2 membrane showing pin fittings that locate L0 to L1 and L1 to L2.

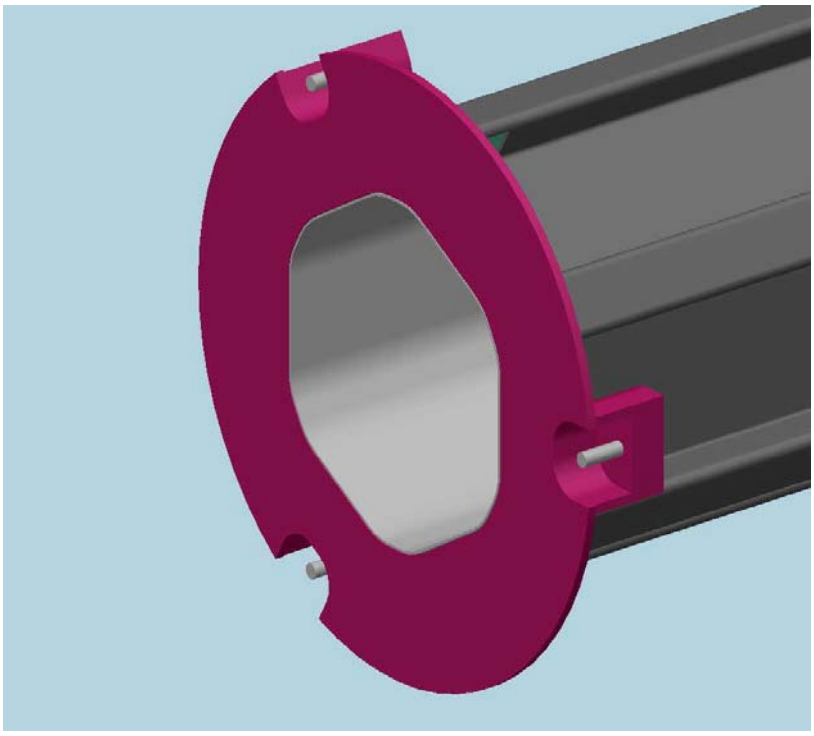


Figure 41: Membrane that connects L0 to L1 at Z=0.

This membrane has precision pin fittings (Figure 40) that locate L0 and L1 to the membrane and to each other (Figure 41). Another set of such pins locates the membrane to the L2/L5 support structure.

At Z=609 mm, the L0 structure is connected to the inner surface of the L1 structure via the L0 hybrid support ring at that location (Figure 42). This connection will also use precision pins so that L0 is located in a precise position within L1. The outer surface of the L1 structure is connected to the L2/L5 structure in a similar way (Figure 42). To avoid any backlash problems, all of these connections will be spring loaded against precision stops.

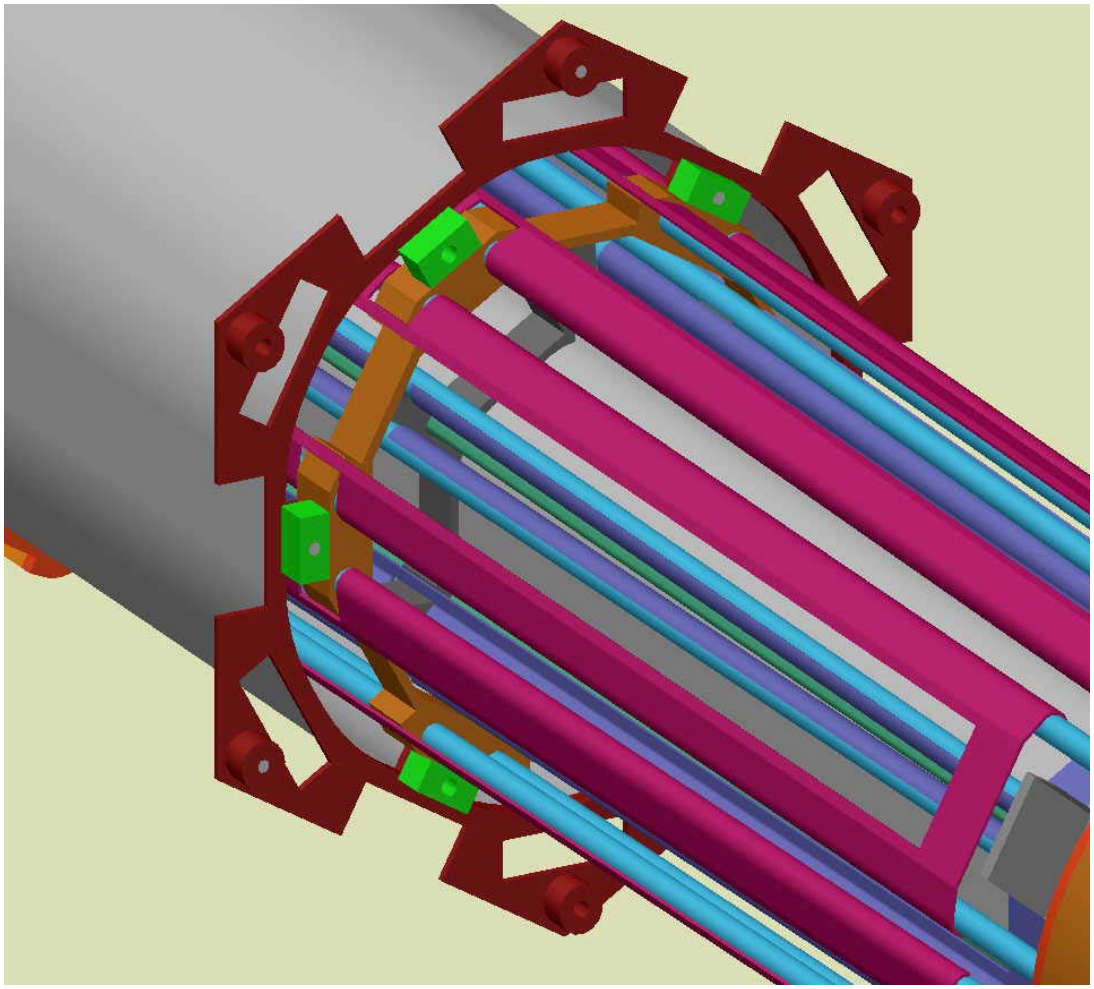


Figure 42: Schematic view of the outer connection from L1 to L2.

4.3.3 FEA analysis of the L0/L1 mechanical structures

4.3.3.1 Mechanical FEA

The high precision required in the L0 and L1 silicon support structures implies that these very light structures must also be very stiff. The design process must be accompanied by detailed structural analysis using FEA methods.

L1 support structure

The current design of the L1 support structure was modeled using the Ansys 6.0 FEA software. The model was generated using the parametric design language in Ansys. This allows the user to readily make changes in the geometry, material properties and loading conditions as the design evolves and as better knowledge of material properties is obtained. The model includes detailed representations of all of the major structural parts. This includes the inner carbon fiber tube, the outer carbon fiber castellation with its cooling tubes, the cooling manifold/bulkhead and the carbon fiber extension from the bulkhead to the end of L1. The orthotropic properties of all of

the fiber structures were determined as discussed below in Section 4.3.4. To keep the model to a manageable size, the stacks of layers involved at the sensors and hybrids (pyrolytic graphite, Kapton, epoxy, silicon and the hybrid substrates) were not modeled in detail. These parts were represented by elements with 'dummy' material properties such that they have equivalent weight and bending stiffness to the actual structures. This was done by modeling short lengths of the silicon and hybrid layers in Ansys and deriving the desired 'dummy' properties from the calculated deflections. The weight of the cooling fluid is accounted for in this step.

The model was loaded by gravity only. Other loads, such as forces from the digital cables and cooling connections, will be added later. Given the symmetry of the structure and the loads, only one half of the structure was modeled (Figure 43). Ansys has a display option that allows one to view the whole structure and this is used in all other figures below. Figure 44, Figure 45 and Figure 46 show details of the element structure at various places in the model.

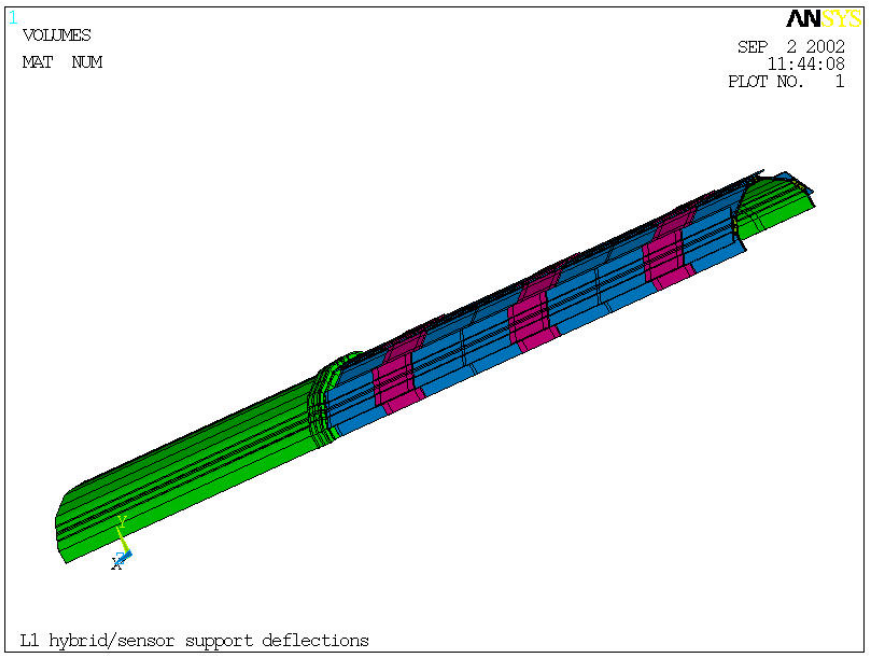


Figure 43: View of the actual model (volumes shown) of the L1 structure.

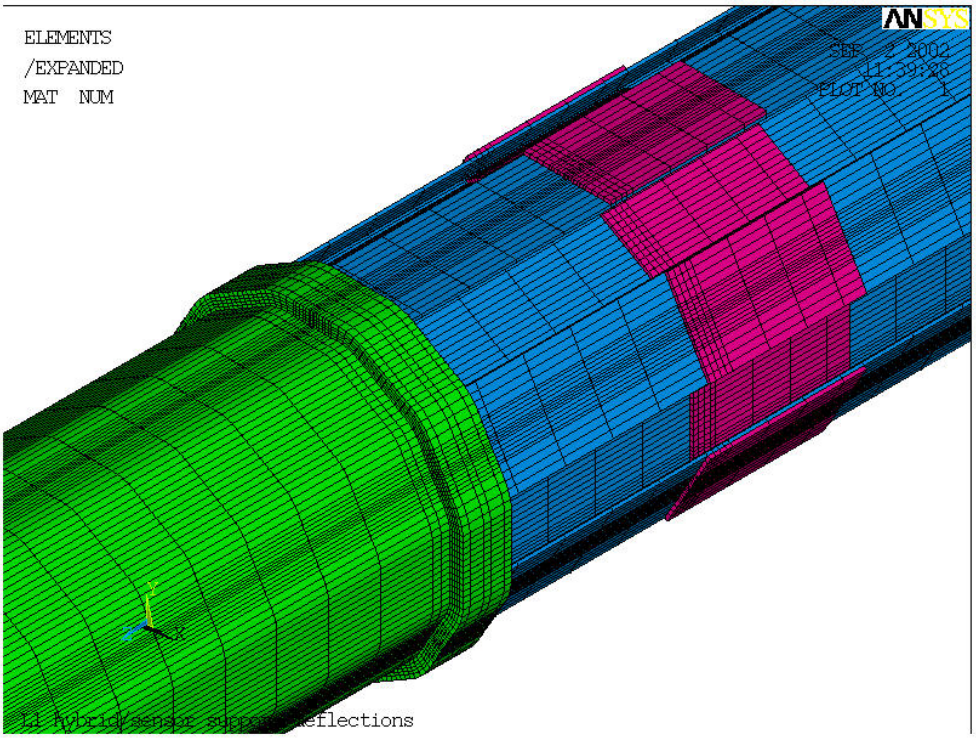


Figure 44: Element structure at the cooling manifold/bulkhead.

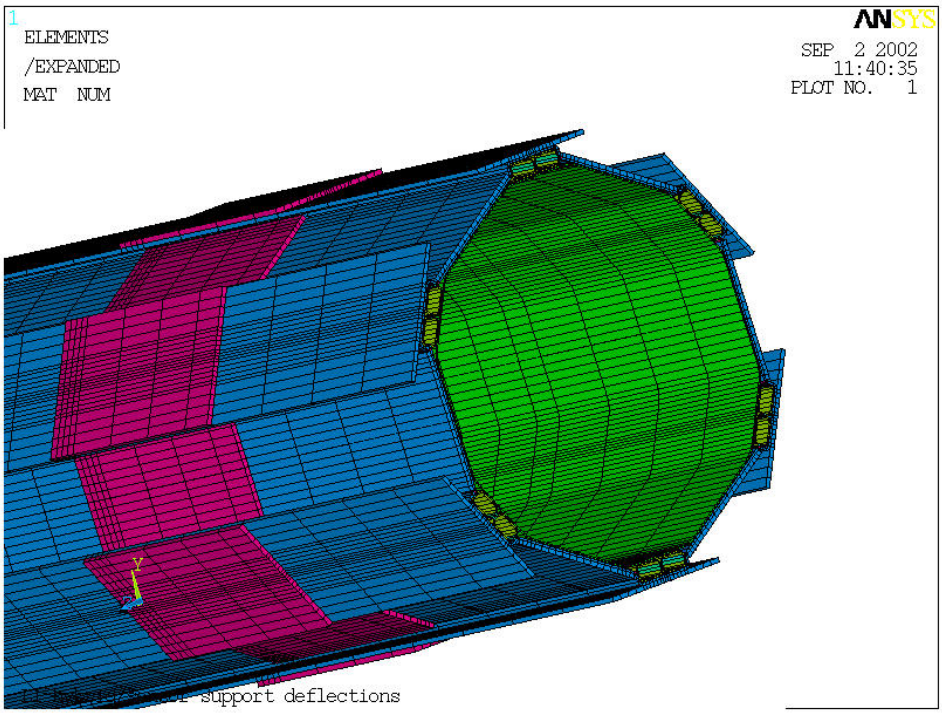


Figure 45: Element structure at Z=0.

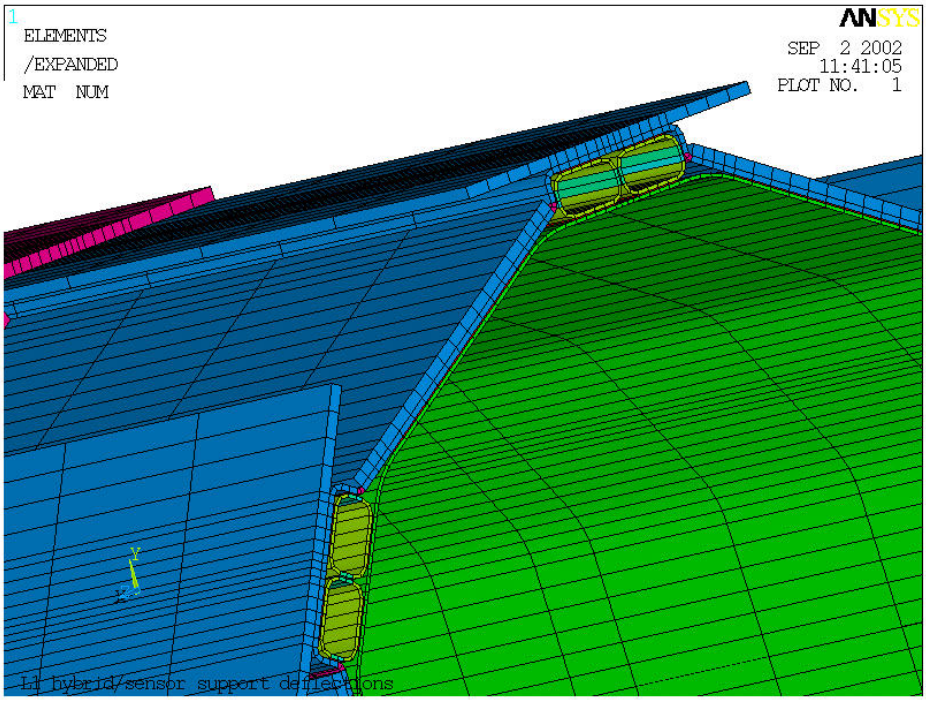


Figure 46: Elements at Z=0 showing details of the cooling tubes.

The deflection of the structure due to its own weight is shown in Figure 47.

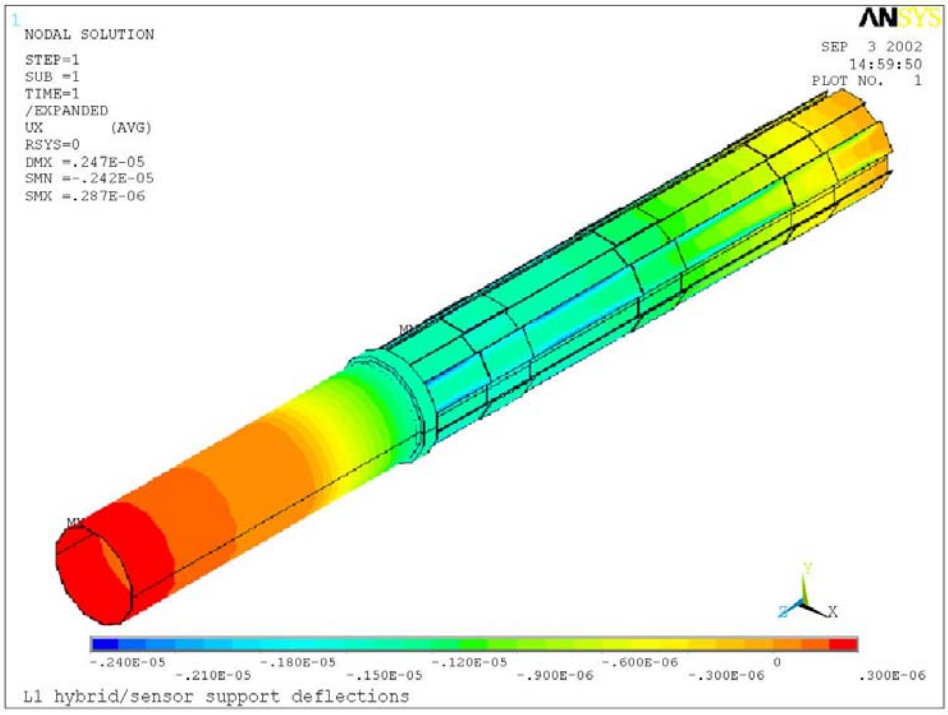


Figure 47: Deflection of the L1 support structure.

The maximum sagitta of the main part of the structure is only 1.55 μm.

L0 support structure

Calculations similar to those done for L1 show that the gravitational deflection of the L0 support structure is well within the required tolerance. In the sensor region, the maximum deflection is less than 6 μm as seen in Figure 48.

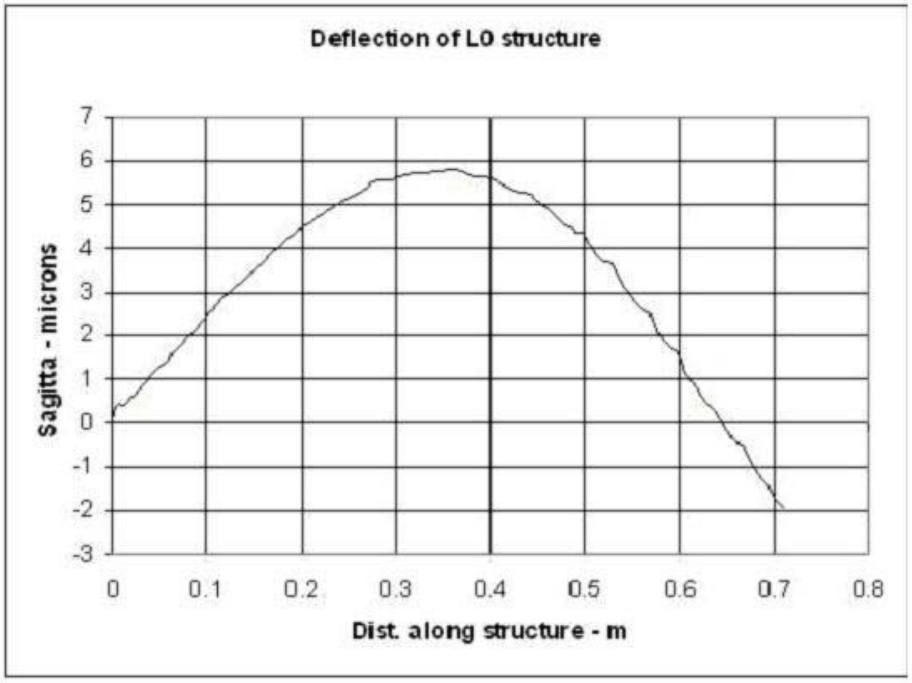


Figure 48: Deflection of L0 support structure.

4.3.3.2 Thermal FEA

L1 support structure

In L1, the hybrids with the heat generating SVX4 chips are mounted on top of the silicon sensors.

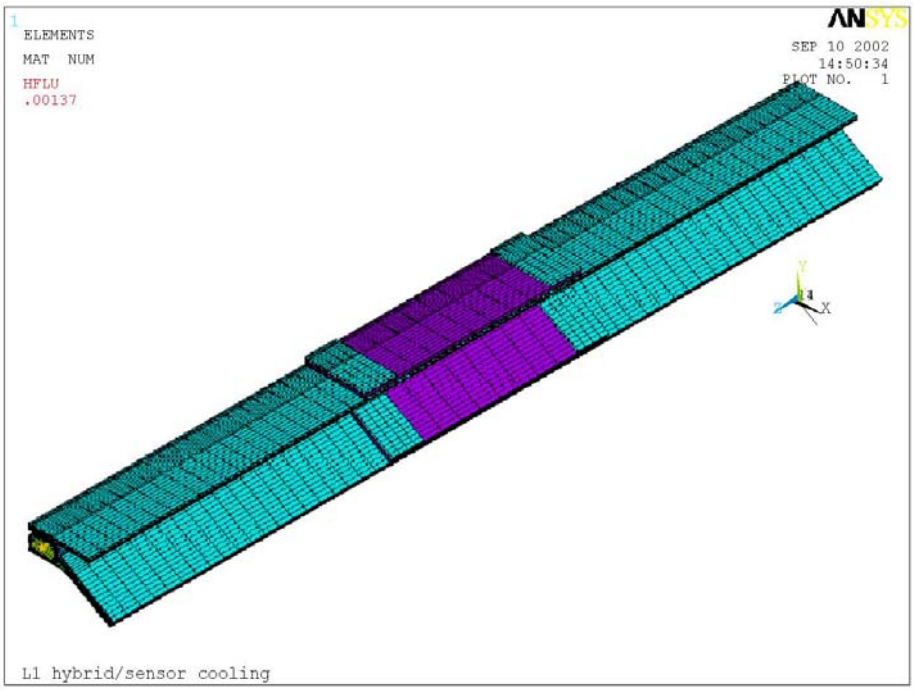


Figure 49: Thermal FEA model of L1.

A very detailed model of one twelfth of the azimuth of the L1 structure was built using Ansys 6.0 for one sensor/hybrid module consisting of two sensors with their associated hybrid. This covered one half of the width of each of the L1a and L1b layers of modules and is shown in Figure 49.

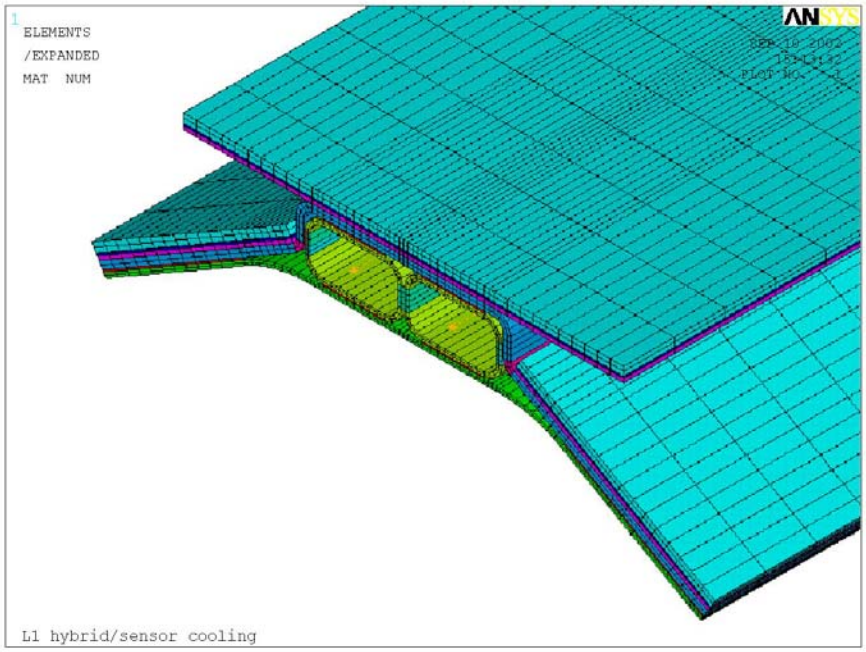


Figure 50: Close up of end of model showing the cooling tubes.

The close up view seen in Figure 50 shows the details of the modeling of the cooling tubes. The line elements within each tube are used to model the flow of and heat transfer to the coolant. The various layers of carbon fiber, epoxy, pyrolytic graphite, Kapton and silicon are modeled in detail. The orthotropic thermal properties of the carbon fiber layers (given in section 4.3.4) are properly accounted for.

Here the layers of epoxy, Kapton, pyrolytic graphite, sensors and the three layers in the hybrid substrate are modeled in detail. Note that the actual model is only one half of that shown in the figures. All views shown use the Ansys capability of reflecting symmetry to generate the more complete views shown.

The thermal loads on the model consisted of the power generated in each hybrid by the SVX4 chips and the coolant flow in the tubes. In the results shown below, the coolant inlet temperature was –15 C and each SVX4 chip generated 0.5 W. The coolant flow velocity was set at 0.1 m/s. This value corresponds to a pressure drop of 1.3 kPa across both tubes. As the model is fully parametric, all of these values as well as the model geometry and material properties can be changed very readily.

The equilibrium temperature of the L1 structure under these conditions is shown in Figure 51. Note that the highest temperature (-1.71 C) is on the SVX4 chips in the L1b layer. .

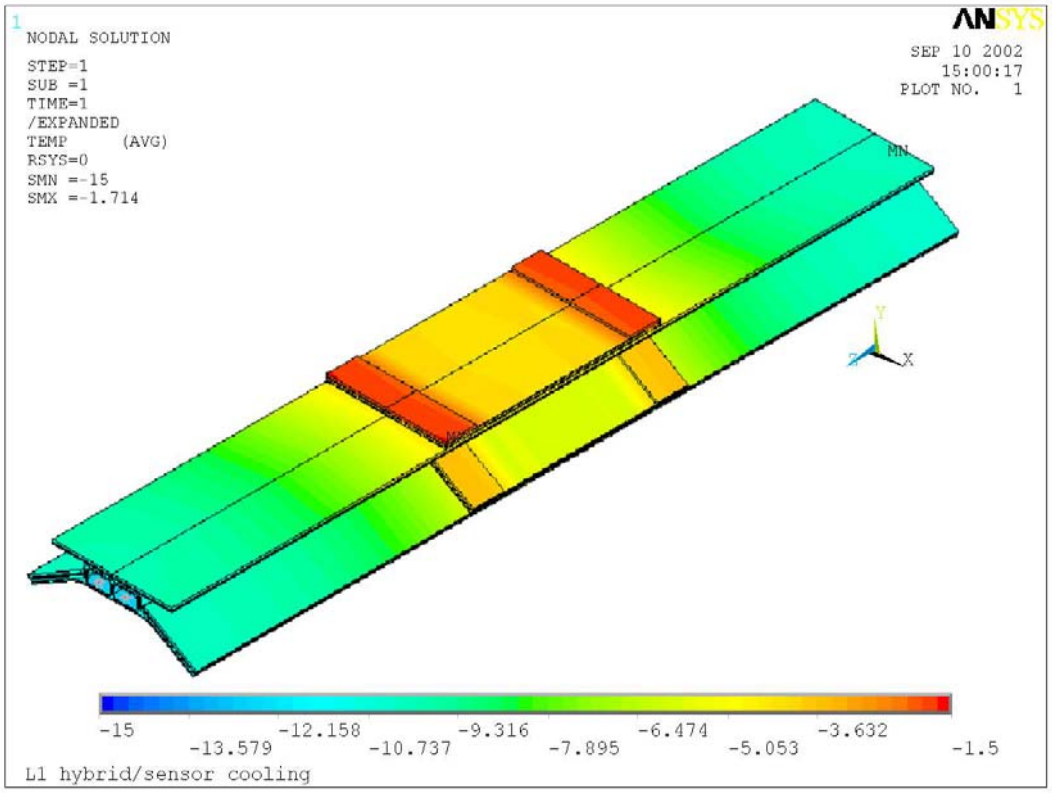


Figure 51: Surface temperature of one set of L1 sensor chips and their hybrid.

The silicon sensor temperatures are shown in Figure 52. The highest temperature is –3.5 C on the L1b layer silicon. The L1a layer is at –5.5 C.

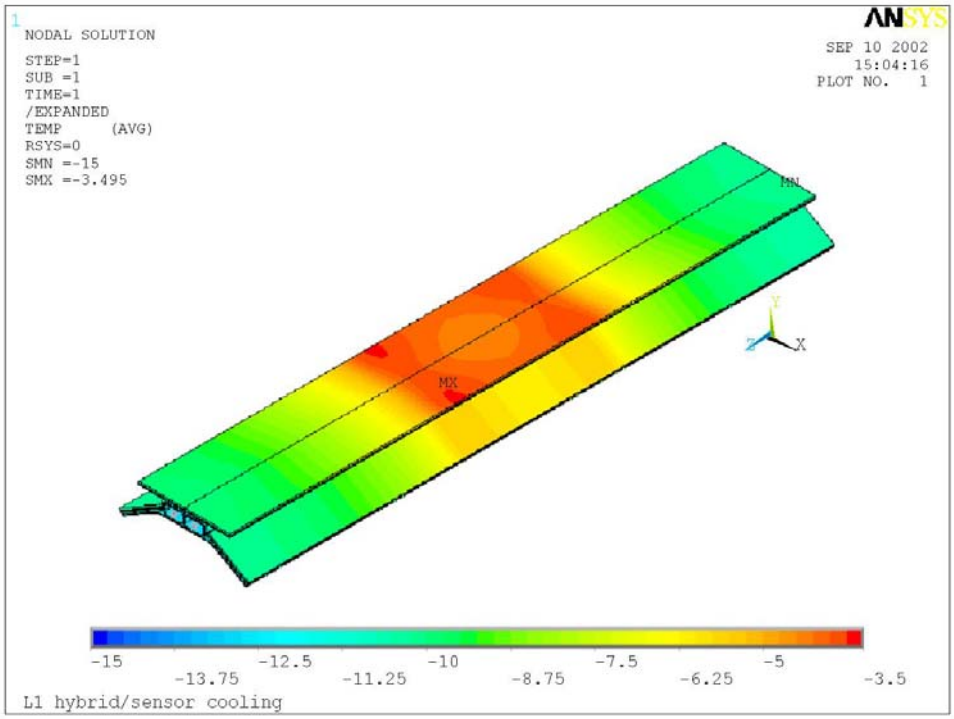


Figure 52: Temperature map showing the silicon sensors

The temperature rise in the coolant is 0.661 C as shown in Figure 53. The temperature change shown is for flow in one tube, 160 mm in length. This is because only one half of the width of the sensors is actually used in the model. Also the length of the section modeled is only one third of the total length and heat load of the full structure. . The actual heat generated is, thus, six times the values given above. The overall temperature rise in the fluid is also six times the above values. In practice, fluid enters along one edge and leaves in the opposite direction along the other. The cooling tubes within the castellations run very close to each other but are not in direct contact. The fluid enters on one tube, flows to the end at Z=0, turns around and then flows in the opposite direction to the incoming flow. The possible heat transfer between the tubes was studied and found to be negligible.

As the silicon sensors age in use, they generate more heat. A thermal load of 0.1 W per chip was added to the model to simulate this. As shown in Figure 54, this load increases the maximum sensor temperature to –2.0 C.

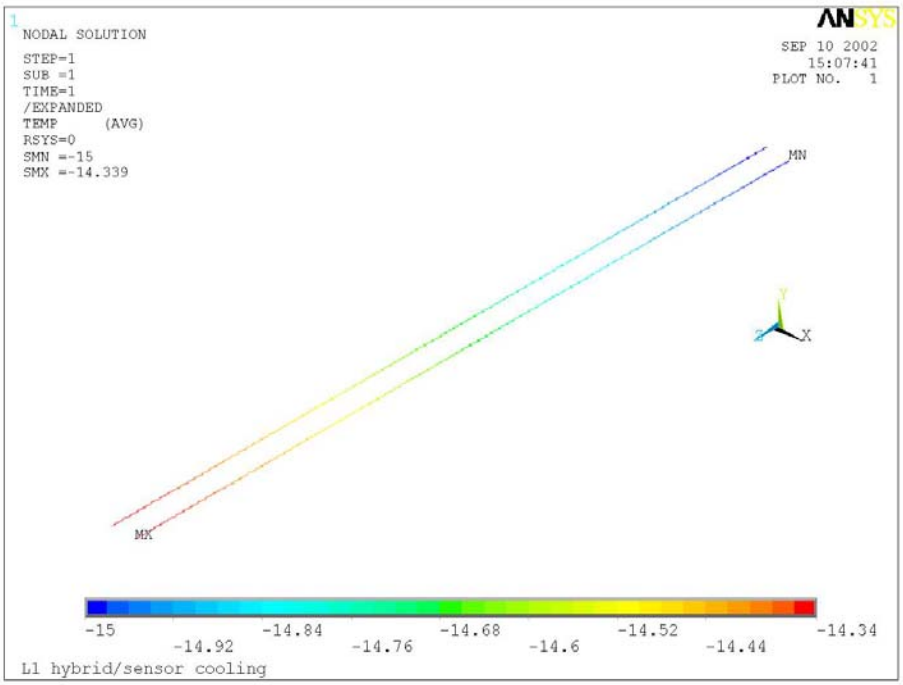


Figure 53: Temperature rise in the coolant lines.

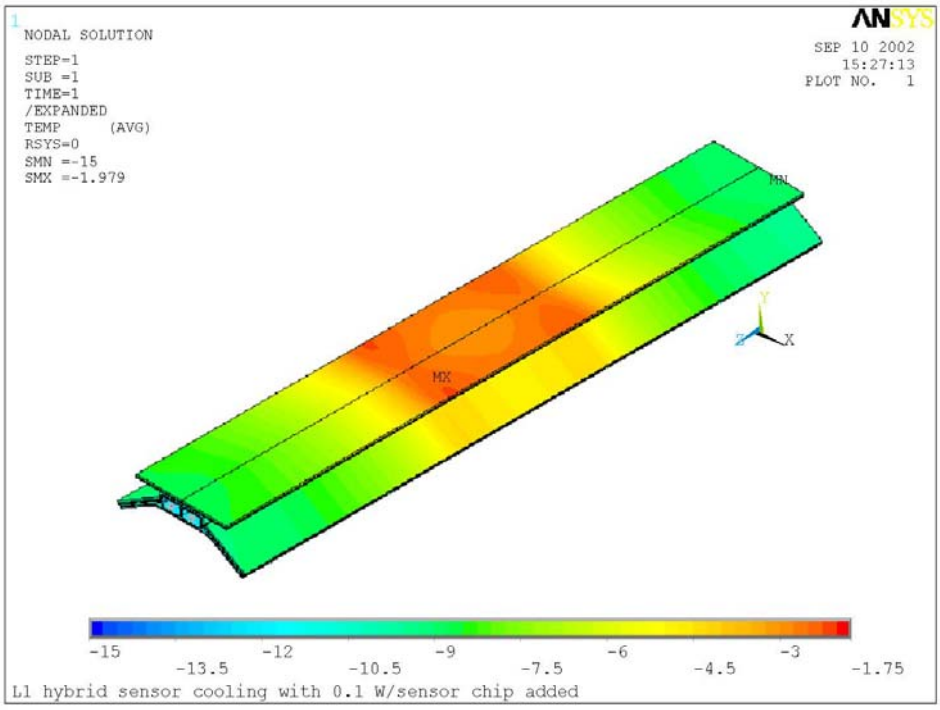


Figure 54: Sensor temperature with 0.1 W heat load applied to each silicon sensor chip.

L0 support structure

Simple 2-d thermal FEA analysis was used in the design phase for the L0 cooling system. This showed that the adopted design has more than adequate cooling capacity. The L0 silicon sensors are cooled by a separate cooling circuit from their associated hybrids and are thus, easy to cool.

4.3.3.3 Conclusions

The deflection results obtained for L1 show that this structure is extremely stiff and that the mechanical design has a large design reserve. For L0, a study of the stiffness of the main structure shows that the gravitational sag is very similar to that seen in the L1 FEA calculations, well within the allowed tolerance.

The L1 thermal results show that, prior to irradiation, with the coolant inlet temperature at –15 C, the maximum temperature seen on the silicon sensors is 3.5 C. With irradiation, this increases to –2.0 C.

Thermal results obtained on some simple 2-d FEA studies on L0 were used during the design phase for the L0 cooling system. These showed that the design was capable of easily meeting the requirement that the maximum silicon temperature be maintained below -10 C.

4.3.4 Properties of Carbon Fiber Composites

A detailed FEA analysis has been performed to support the design of the L0/L1 support structure. The validity of this analysis hinges on an accurate *a priori* knowledge of the elastic and thermal properties of the composite laminates used within the structure. Laminates with different stacking sequences will be used and, therefore, properties will vary substantially from one laminate to the next.

Elastic and thermal properties of a given laminate have been predicted on the basis of standard classical lamination theory (CLT). This requires that the following elastic and thermal properties for unidirectional laminates must be known:

- E_1 and E_2 (Young's modulus parallel and perpendicular to the fiber direction)

- ν_{12} (the "major" Poisson ratio)

- G_{12} (the shear modulus)

- α_1 and α_2 (thermal expansion coefficients parallel and perpendicular to the fiber direction), and

- K_1 and K_2 (thermal conductivity parallel and perpendicular to the fiber direction)

Once these properties are known, CLT can then be used to predict the equivalent properties for a composite laminate of any desired stacking sequence. A series of tests was performed to

demonstrate the accuracy of CLT predictions. Both elastic and thermal properties were considered. First, the elastic properties E_1, E_2, ν_{12}, and G_{12} were measured for a K13C/epoxy pre-preg. E_1 and ν_{12} were measured using a $[0]_6$ tensile specimen and E_2 was measured using a $[90]_6$ tensile specimen, following ASTM test standard D3039[20]. G_{12} was inferred from E_x and ν_{xy} measured for a $[45/-45]_s$ tensile specimen, following ASTM test standard D3518[21]. Experimental results are summarized in Figure 55 through Figure 59. Measured values were:

$E_1 = 410$ GPa $E_2 = 5.56$ GPa $\nu_{12} = 0.39$ $G_{12} = 4.10$ GPa

Shear modulus $G_{12} = E_x/2(1 + \nu_{xy})$

The effective axial stiffness (E_x) and major Poisson ratio (ν_{xy}) were then measured for a $[0/20/-20]_s$ laminate. Experimental results are summarized in

Figure 60 and Figure 61.

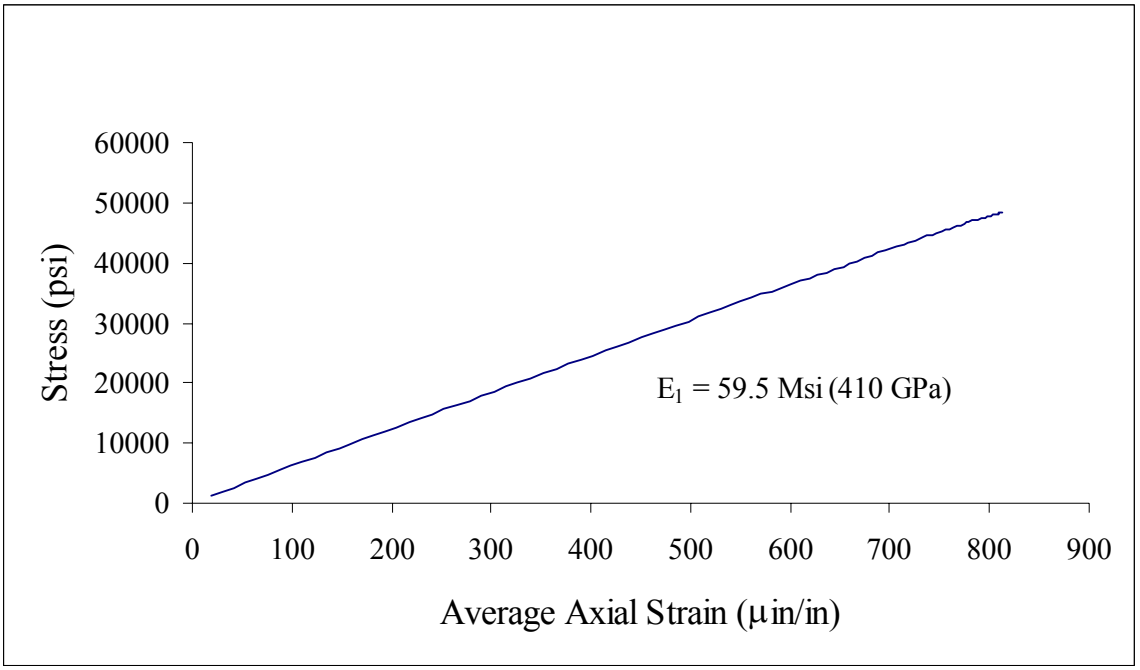


Figure 55. Modulus E_1 measured using a $[0]_6$ K13C/epoxy laminate.

[20] ASTM Standard D3039/D3039M "Standard Test Method for Tensile Properties of Polymer Matrix Composite Materials", published by American Society for Testing and Materials, www.astm.org

[21] ASTM Standard D3518/D3518M-94 "Standard Test Method for In-Plane Shear Response for Polymer Matrix Composite Materials by Tensile Test of a +/- 45 Laminate", published by American Society for Testing and Materials, www.astm.org

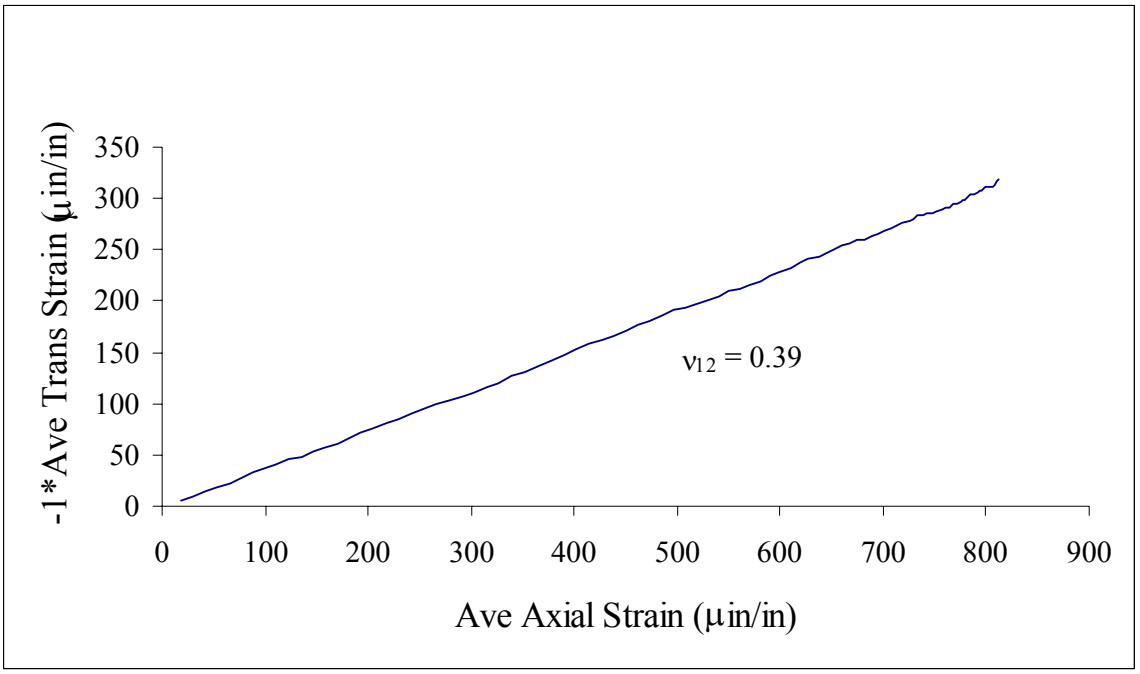


Figure 56. Poisson ratio ν_{12} measured using a $[0]_6$ K13C/epoxy laminate.

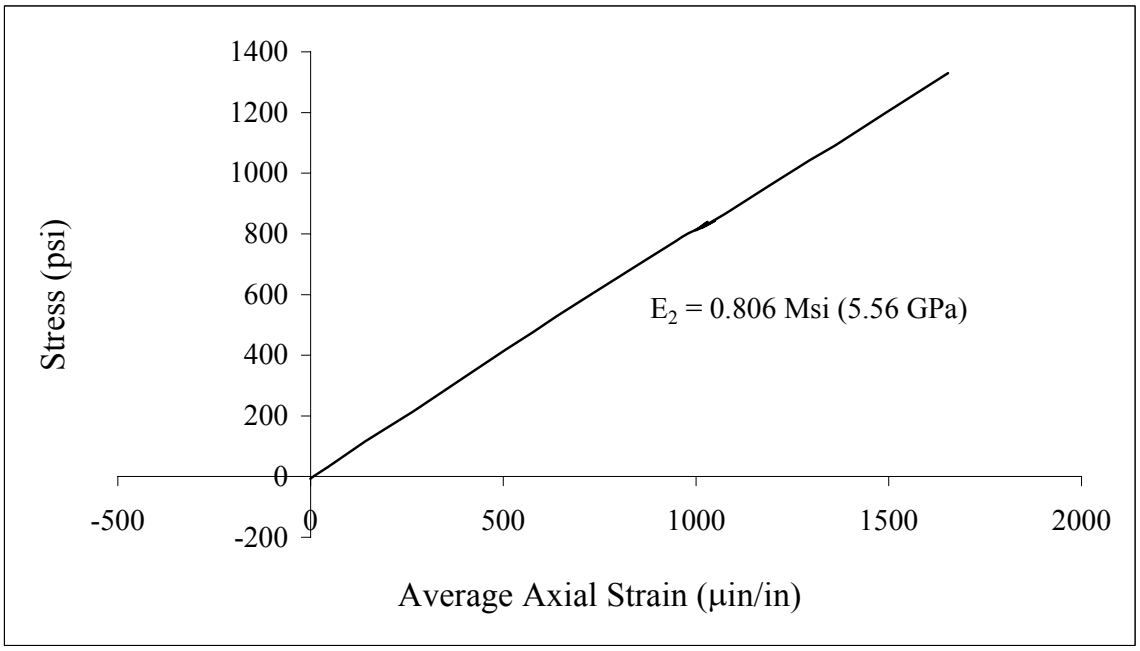


Figure 57. Modulus E_2 measured using a $[90]_6$ K13C/epoxy laminate.

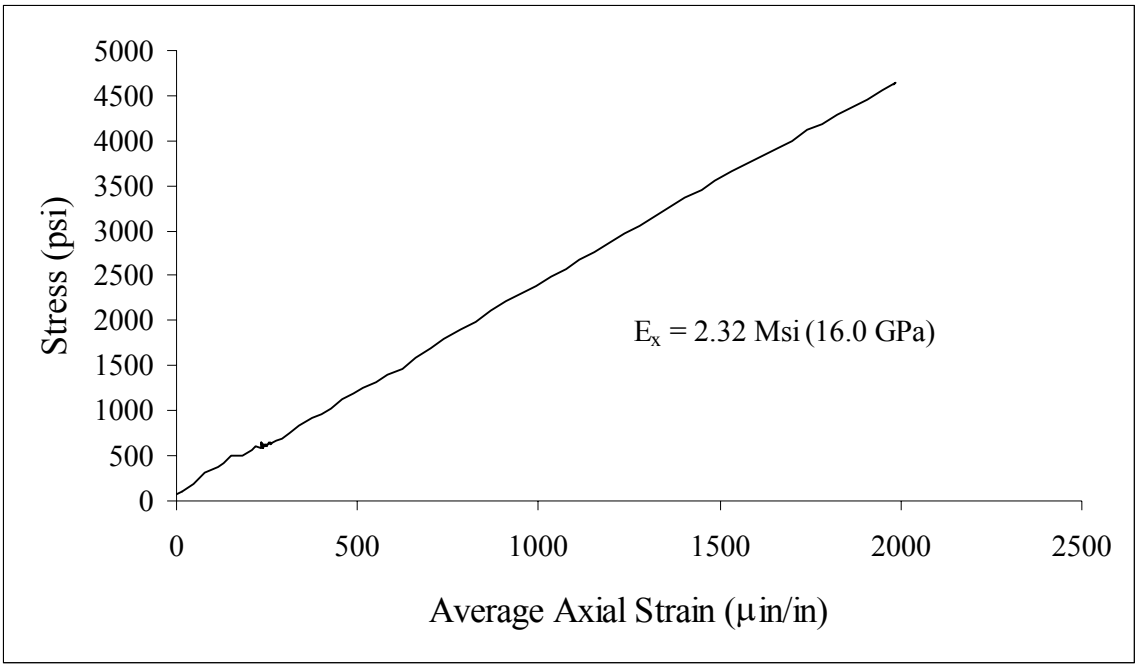


Figure 58. Modulus measured for a [45/-45]$_s$ tensile specimen.

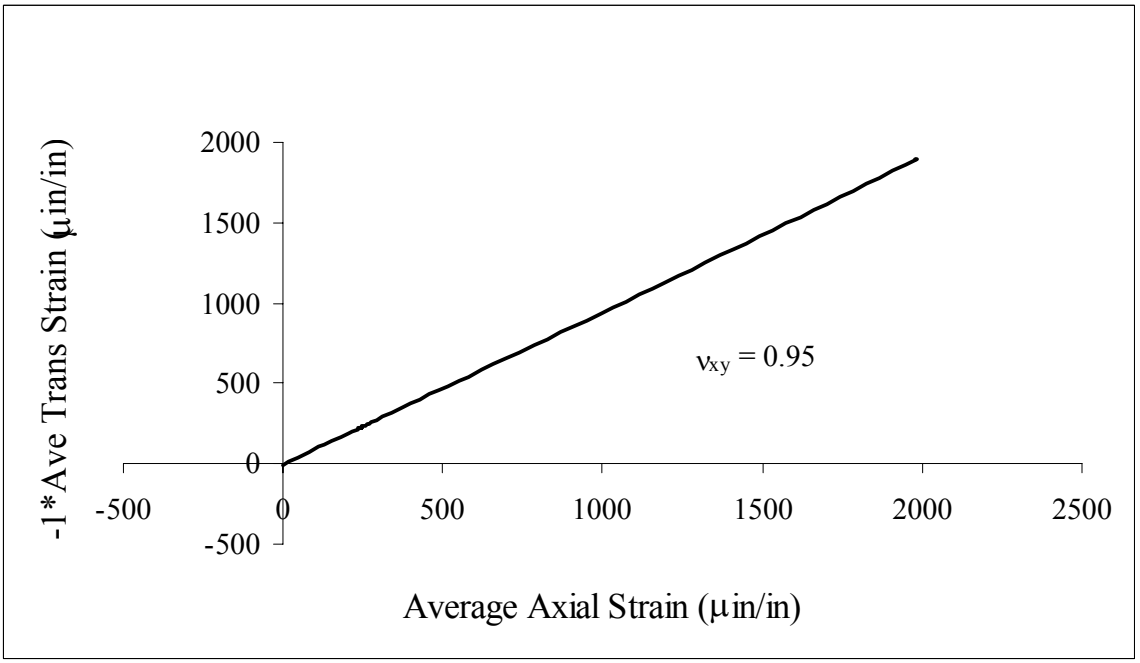


Figure 59. Poisson ratio measured for a [45/-45]$_s$ tensile specimen.

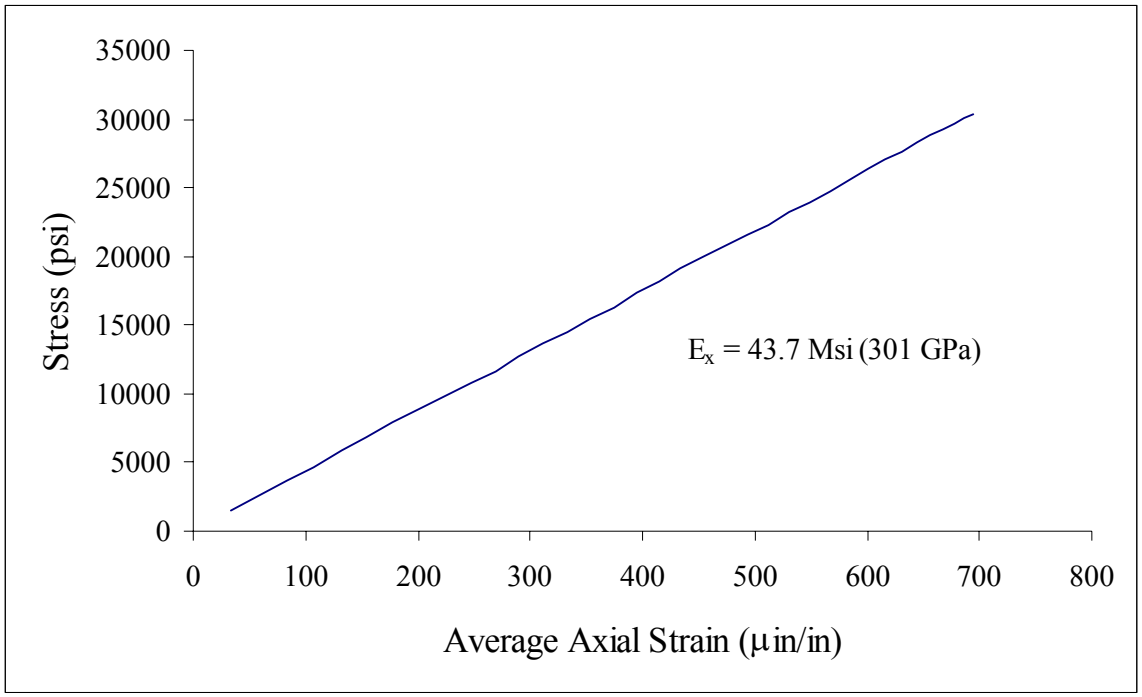


Figure 60. Modulus E_x measured for a $[0/20/-20]_s$ K13C/epoxy laminate

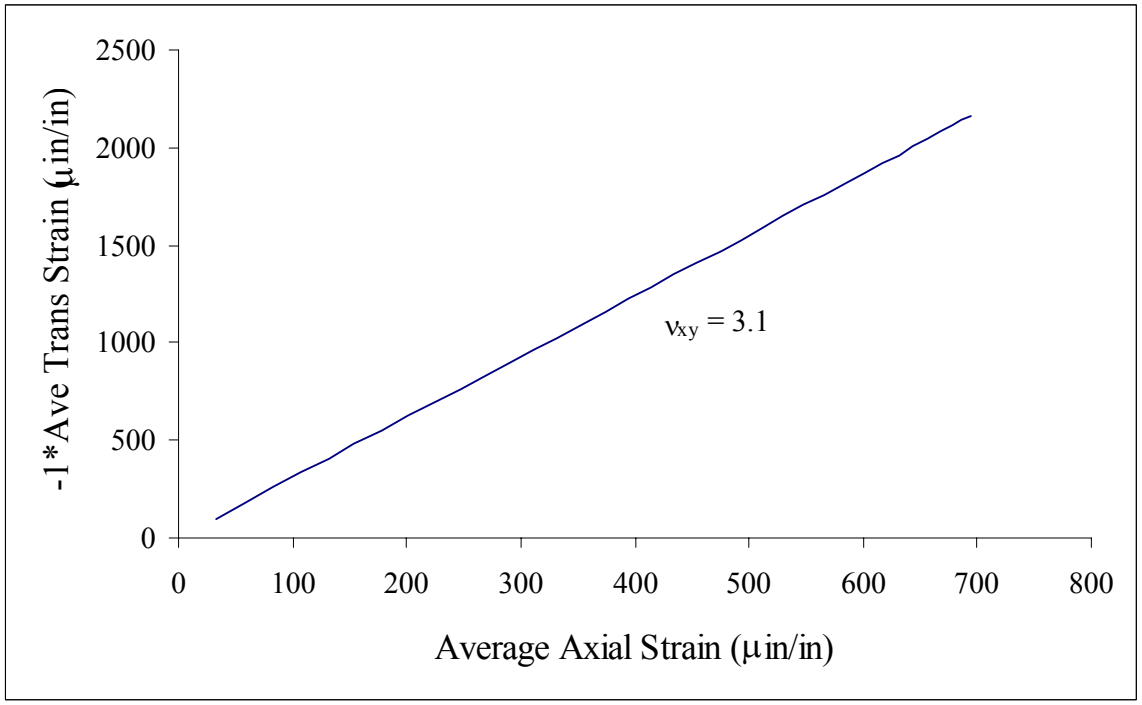


Figure 61. Poisson ratio ν_{xy} measured for a $[0/20/-20]_s$ K13C/epoxy laminate.

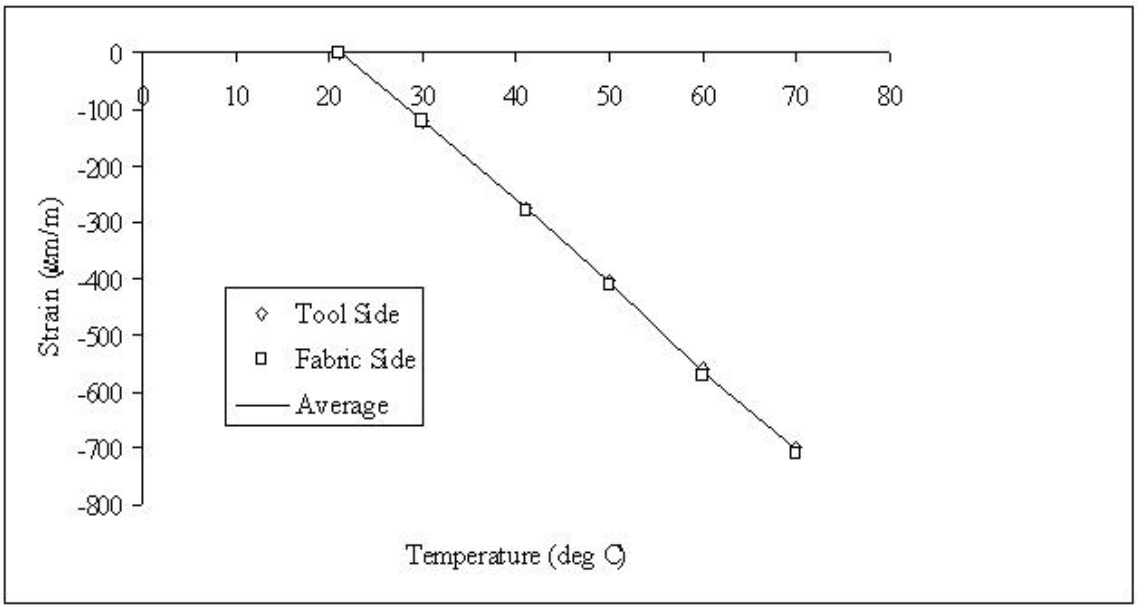


Figure 62. Thermal strains used to infer α_1 for K13C/Epoxy. Slope implies α_1 = -3.7μm/m-C.

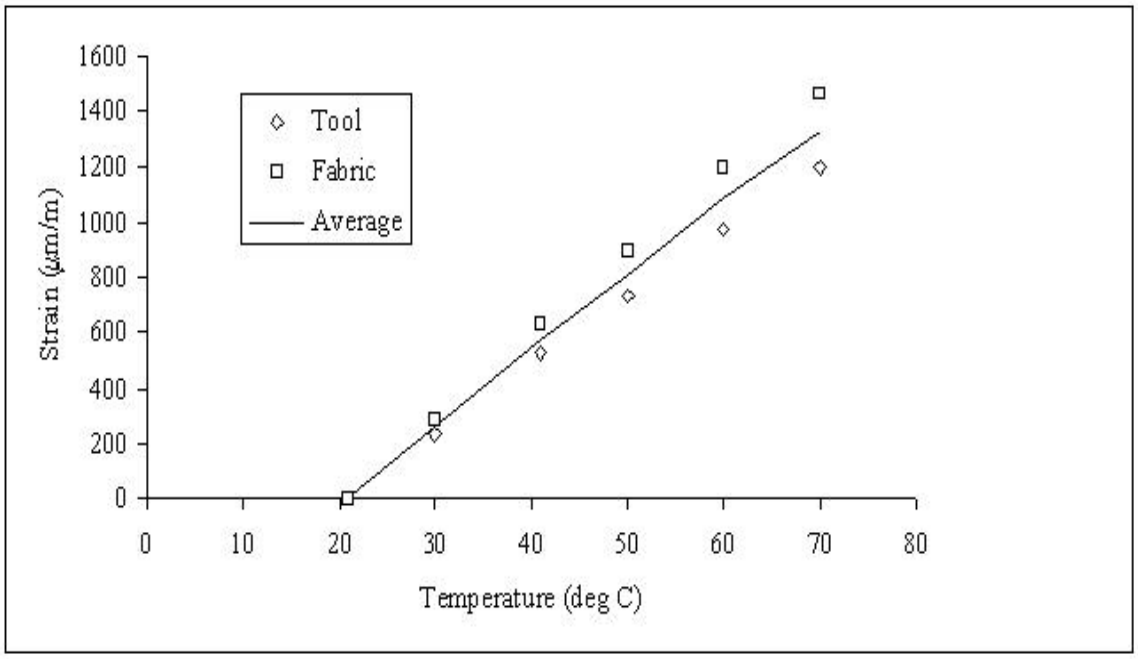


Figure 63. Thermal strains used to infer α_2 for K13C/Epoxy. Slope implies α_2 = 38.0μm/m-C.

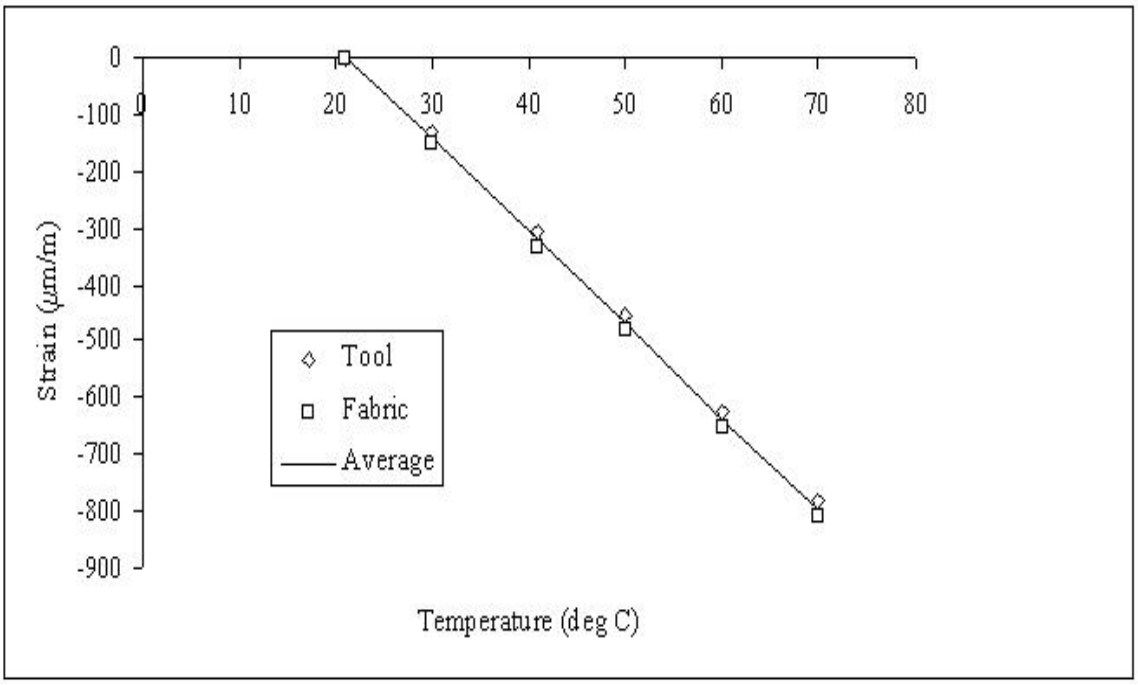


Figure 64. Thermal strains used to infer α_x for a [0/20/-20]s K13C/Epoxy laminate. Slope implies α_x = -5.5 μm/m-C.

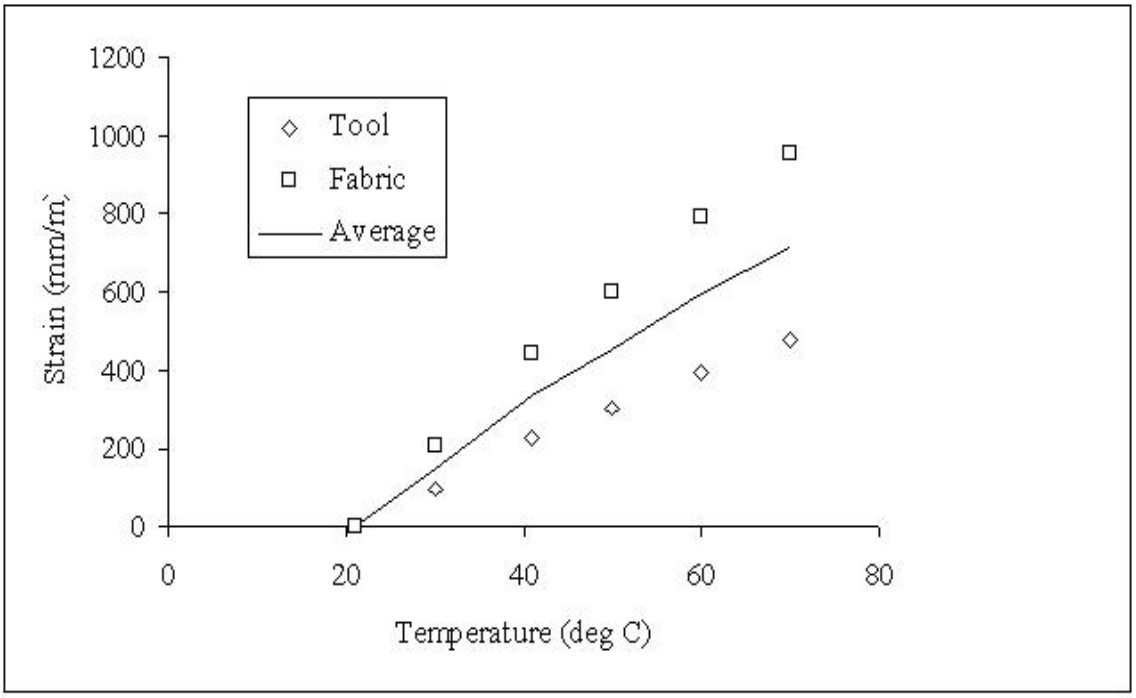


Figure 65. Thermal strains used to infer α_y for a [0/20/-20]s K13C/Epoxy laminate. Slope implies α_y = -5.5 μm/m-C.

Properties predicted for this stacking sequence using CLT are compared to measured values in Table 10. Excellent agreement was achieved. Notice that an unusually large and non-intuitive Poisson ratio (ν_{xy} = 3.1) was measured for the $[0/20/-20]_s$ laminate and correctly predicted by CLT.

Thermal expansion coefficients α_1 and α_2 were also measured for the same K13C/epoxy material system, following an industry test standard[22]*. Experimental results are summarized in* Figure 62 *and*

Figure 63. Thermal expansion coefficients were measured as:

α_1 = -3.7 μm/m-C α_2 = 38.0 μm/m-C

Effective axial and transverse thermal expansion coefficients (α_x and α_y) were then measured for a $[0/20/-20]_s$ laminate. Experimental results are summarized in Figure 64 and Figure 65. Thermal expansion coefficients predicted for this stacking sequence using CLT are compared to measured values in Table 10. As before excellent agreement was achieved, further demonstrating the accuracy of CLT

[22] "MM Tech Note TN-513, "Measurement of Thermal Expansion Coefficient Using Strain Gages", available from Vishay Measurements Group, www.vishay.com

Table 10. Comparison between measured and predicted properties of a $[0/20/-20]_s$ K13C/epoxy laminate.

	E_x (GPa)	ν_{xy}	α_x (μm/m-C)	α_y (μm/m-C)
Measured	301	3.1	-5.5	25.4
Predicted	265	3.0	-5.9	24.7

The preceding results show that CLT can be used to predict the elastic and thermal properties of a composite laminate with arbitrary stacking sequence. The demonstrated agreement between measurement and prediction is important, since it implies that the detailed FEA analysis of the L0/L1 support structures, which involve composite laminates with several different stacking sequences, can be based on laminate properties predicted using CLT.

As previously mentioned, the L0/L1 support structure will be produced using laminates with several different stacking sequences. Properties of the laminates involved are presented in Table 11 and Table 12. These properties were obtained based on CLT, and were used during the detailed FEA analyses of the L0/L1 support structures.

Table 11. Properties of Laminates Based on K13C/Epoxy Prepreg.

Lay-up	E_{axial} (E_y)	E_{circ} (E_x)	E_{rad}(E_z)	G_{yx}	G_{yz}	G_{xz}	ν_{yx}	ν_{yz}	ν_{xz}
	GPa	GPa	GPa	GPa	GPa	GPa			
$[0/20/-20]_s$	265.1	7.51	5.96	31.4	3.99	2.83	2.95	-.712	.379
$[0/25/-25]_s$	213.7	10.0	6.18	42.8	3.94	2.88	2.70	-.624	.362
$[0/90/]_s$	208.2	208.2	6.67	4.10	3.41	3.41	.0104	.477	.477
$[45/-45/]_s$	15.78	15.78	6.67	103.1	3.41	3.41	.925	.0362	.0362

Lay-up	α_{axial} (α_y)	α_{circ} (α_x)	α_{rad}(α_z)	K_y	K_x	K_z
	μm/m-C	μm/m-C	μm/m-C	W/m-K	W/m-K	W/m-K
$[0/20/-20]_s$	-5.80	24.86	44.26	343.1	29.69	.726
$[0/25/-25]_s$	-5.93	16.63	47.69	327.9	44.95	.726
$[0/90/]_s$	-2.93	-2.93	54.49	186.4	186.4	.726
$[45/-45/]_s$	-2.93	-2.93	54.49	186.4	186.4	.726

Table 12. Laminates Based on K139/Epoxy Prepreg.

Lay-up	E_{axial} (E_y)	E_{circ} (E_x)	E_{rad}(E_z)	G_{yx}	G_{yz}	G_{xz}	ν_{yx}	ν_{yz}	ν_{xz}
	GPa	GPa	GPa	GPa	GPa	GPa			
$[0/20/-20]_s$	243.2	6.09	4.51	29.52	3.53	2.786	3.29	-.871	.379
$[0/25/-25]_s$	196.2	8.50	4.68	40.41	3.50	2.82	2.89	-.718	.362
$[0/90/]_s$	196.9	196.9	5.01	3.60	3.16	3.16	.0078	.464	.464
$[45/-45/]_s$	13.9	13.9	5.01	97.7	3.16	3.16	.930	.0327	.0327

Lay-up	α_{axial} (α_y)	α_{circ} (α_x)	α_{rad}(α_z)	K_y	K_x	K_z
	μm/m-C	μm/m-C	μm/m-C	W/m-K	W/m-K	W/m-K
$[0/20/-20]_s$	-5.97	21.2	42.7	116.3	10.5	.726
$[0/25/-25]_s$	-6.01	13.1	46.0	111.2	15.65	.726
$[0/90/]_s$	-3.52	-3.52	51.85	63.41	63.41	.726
$[45/-45/]_s$	-3.52	-3.52	51.85	63.41	63.41	.726

4.3.5 Fabrication Techniques

The L0/L1 support structure is fabricated using pre-preg tape and hand-lay-up, as described below.

4.3.5.1 Support Structure Fabrication

The support structure shells are fabricated by wrapping carbon fiber pre-preg material around mandrels that are machined to the specified cross-sectional dimensions. The outer, castellated shells are 6 ply lay-ups, with fiber orientations of $[0°/20°/-20°]_s$. The inner shells are 4 ply lay-ups in the sensor regions, with fiber orientations of $[0°/90°]_s$. To increase the stiffness of the inner shells, an additional 4 plies are added outside of the sensor regions, also at $[0°/90°]_s$. A cross-section of the L0 shell assembly is shown in Figure 66.

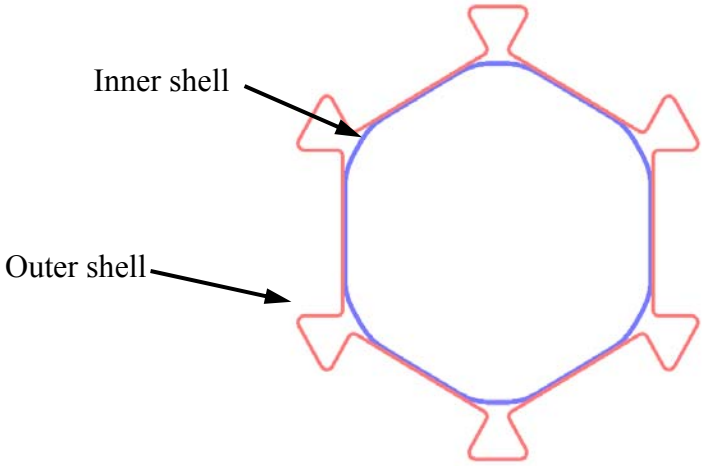


Figure 66. L0 shell assembly

Standard vacuum/autoclave procedures are employed in the lay-up of the carbon fiber shells, as recommended by the material manufacturer. The following section describes the various steps involved in the lay-up of an L0 castellated outer shell. Similar techniques are used for the L0 inner shell, as well as the L1 shells. Note that the lay-up shown is a design prototype and is only 1/3 of the actual length.

Material Preparation

The K13C2U pre-preg must be stored in an airtight bag and kept below 10° F when not in use. The roll of material is removed from the freezer and allowed to reach room temperature prior to handling. The thawed roll is then opened, and the various plies are measured and cut to size. Reference lines are transferred to the backing paper to aid in fiber orientation during lay-up. The cut parts are placed in an airtight bag, and returned to the freezer until ready for lay-up.

Mandrel Preparation

The mandrel is first lightly polished with a fine abrasive pad to remove any residual material left behind from previous lay-ups. The mandrel is then cleaned with soap and water and blown dry with dry air or nitrogen. A final cleaning is done using pure ethanol, followed by the application of 2-3 coats of a water-based, non-silicone mold release, which is allowed to air dry at room temperature. Finally, the mandrel is heated to 80° F immediately prior to material lay-up. This is done to promote adhesion between the mandrel and the first layer of pre-preg. The prototype castellated mandrel is shown in Figure 67.

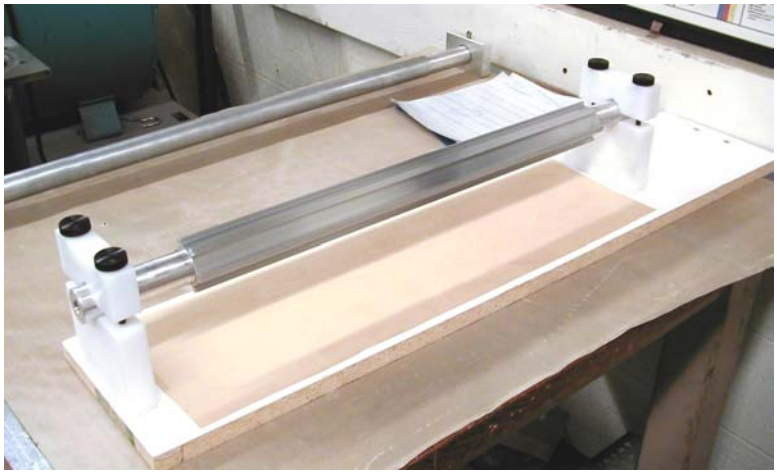


Figure 67. Castellated Mandrel

Material Lay-up

To preserve the integrity of the delicate, thin ply material, the backing paper is pre-released then lightly reattached for handling and fiber orientation. Once the layer is properly configured to the first set of mandrel features, the backing paper is removed and discarded. The first ply will adhere weakly to the mandrel. Subsequent layers will adhere to their previous layers. Wrapping of the first ply [0°] to the castellated mandrel is shown in Figure 68.

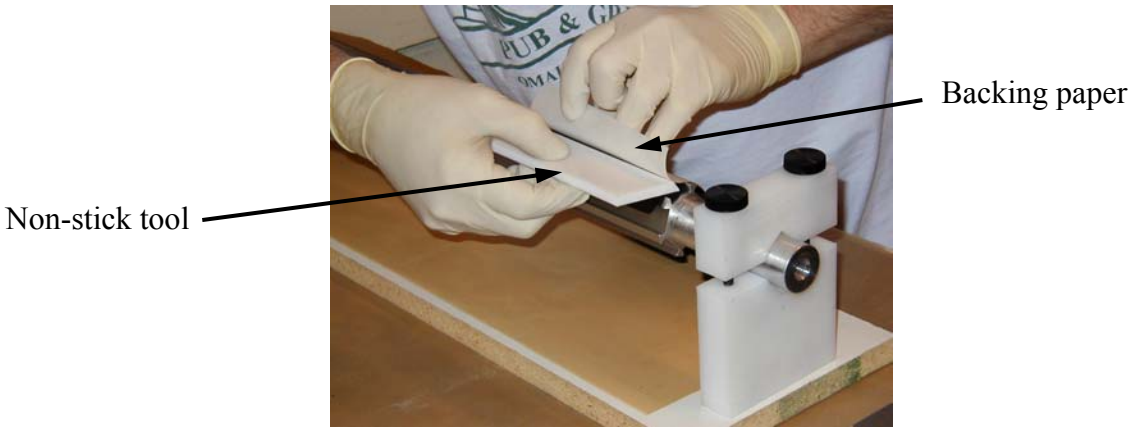


Figure 68. Wrapping first ply

The material is carefully worked around the mandrel using a non-stick tool (Figure 68) to smooth out wrinkles and remove slack. The finished wrap of the first ply is shown in Figure 69.

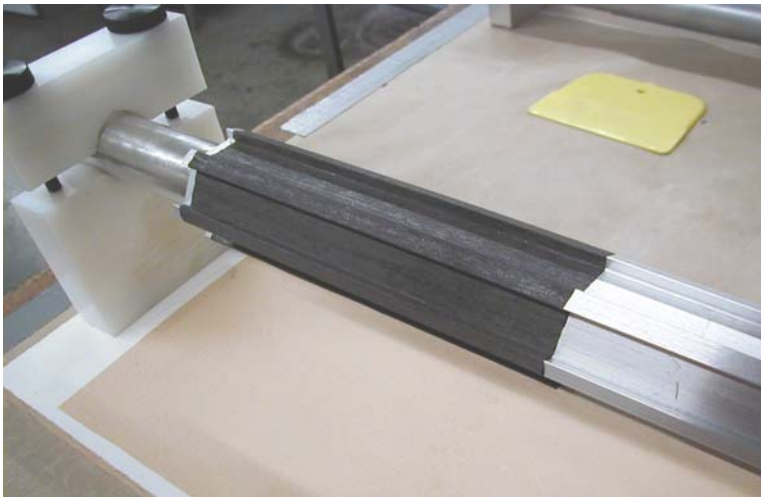


Figure 69. First layer

Since the fiber orientation of the first ply is 0° with respect to the edges of the mandrel features, the fibers are not bent as the material is wrapped around the circumference, and the material conforms to the mandrel with ease. This is not the case with the bias plies, where the fiber orientation is ±20° with respect to the mandrel features. While there is moderate adhesion between plies, the tight bend radii result in a small amount of slack material in the finished wrap of each bias ply. This slack must be removed prior to the cure to avoid, 1) voids in the cured material caused by trapped air, and 2) surface wrinkles and broken fibers created as the slack material is forced against the mandrel. Therefore, it is necessary between each bias ply to install the soft outer mold system (Figure 70), place the lay-up in a vacuum bag, and apply a vacuum for 5 minutes (a process known as "intermediate de-bulking").

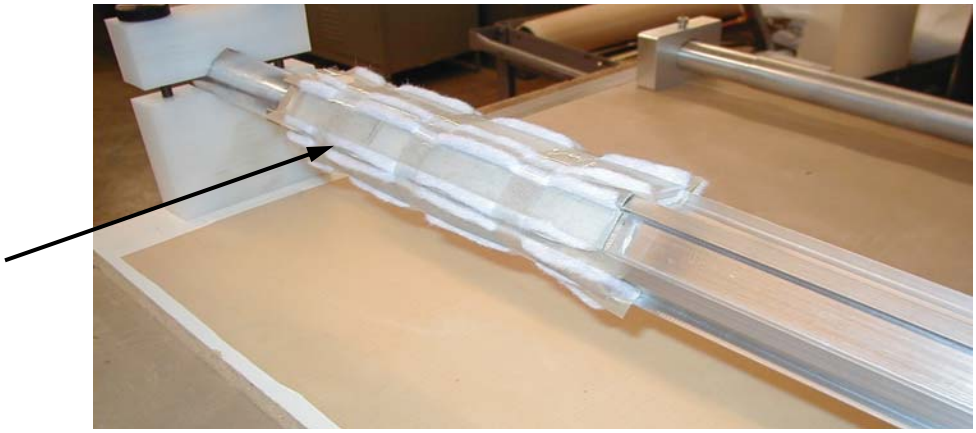


Figure 70. Soft outer mold system

Soft Outer Mold System

The castellated mandrel provides a precise tool surface for the inside surface of the shell during the cure. Outer surface consistency and wall thickness precision are achieved by uniformly compressing the pre-preg lay-up between the mandrel and a series of pressure segments. Force is

applied using a combination of vacuum bagging and external air pressure. The pressure segments consist of precision cast RTV strips wrapped in breather cloth and covered with a layer of porous release ply. The individual segments are wedged between the castellations before installing the vacuum bag Figure 70 A single segment is shown in Figure 71.

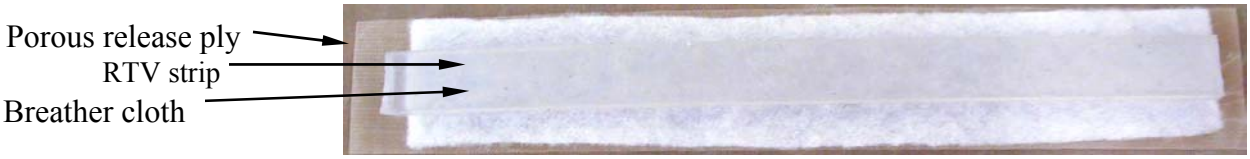


Figure 71. Single segment

Vacuum Bag/Autoclave

Once the outer mold segments are installed to the lay-up, the entire assembly is wrapped in breather cloth, and then thin nylon film. The nylon film is sealed around the mandrel with vacuum tape, creating a "vacuum bag". One end of the mandrel is equipped with a vacuum port. Figure 72 shows the mandrel ready for vacuum testing.

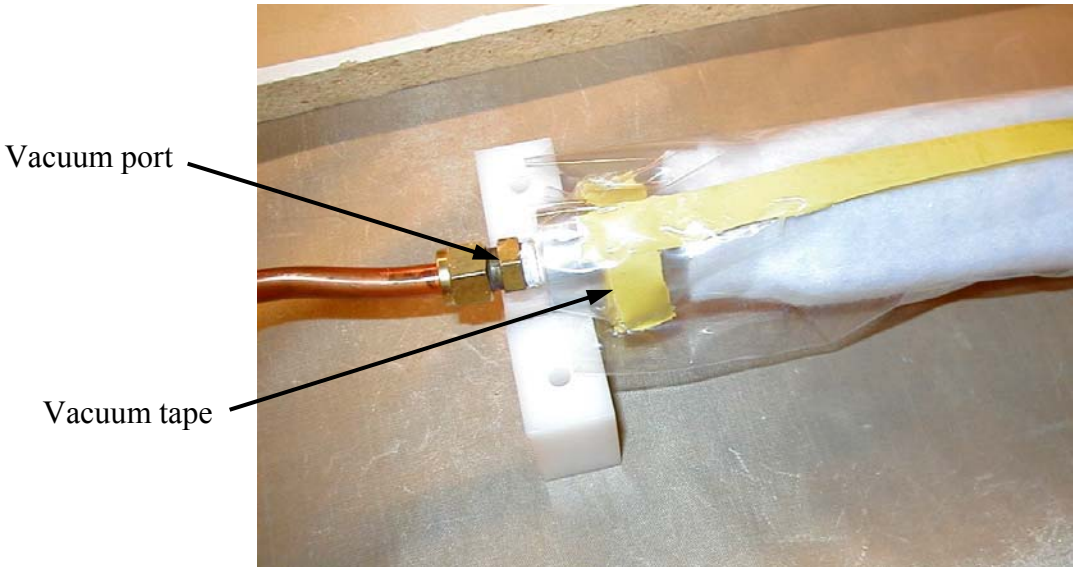


Figure 72. Lay-up ready for vacuum test

Once the lay-up is vacuum tested and found to be leak free, it is loaded into the autoclave, shown in Figure 73.

Figure 73. Loading the autoclave

The autoclave allows for the application of up to 150 psig of external pressure to the lay-up during the cure. Pressure, vacuum and thermocouple connections are made through the cover plate using quick-connect fittings.

Cure Process

The sealed autoclave is loaded into the oven and the pressure, vacuum and thermocouple lines are connected. The vacuum pump and oven heaters are started, and the mandrel temperature is monitored with a digital meter. The external pressure is increased at various temperature intervals:

- no external pressure is applied at startup
- apply 40 psig at 120° F
- increase to 60 psig at 170° F
- increase to 85 psig at 220° F and hold throughout the cure.

The timer is started once the mandrel temperature has stabilized at the recommended cure temperature (250° F for EX1515 resin). After curing for a minimum of 2 hours, the vacuum pump and oven heaters are shut off. The external pressure is maintained until the mandrel temperature has dropped below 160° F.

When the autoclave has cooled sufficiently to allow handling (typically overnight), the mandrel is unloaded and the vacuum bag and soft outer mold materials are removed. The cured shell is then slid from the mandrel. The finished shell is shown in Figure 74.

Figure 74. Prototype L0 outer shell

Quality Assurance

Composites produced as described above have been inspected using optical microscopy. This inspection was performed for two purposes. First, to evaluate whether fibers within the bias plies are fractured during the manufacturing process, particularly in those regions where fibers are required to adopt relatively small radii of curvature. Second, to confirm that the cure cycle results in a composite structure with minimal void content.

An outside vendor performed initial inspections[23]. Many optical micrographs were obtained. Two typical examples are shown in Figure 75 and Figure 76. Figure 75 shows that a few fiber failures did indeed occur in regions of small radii of curvature. However, these fiber fractures are not particularly localized and are not expected to degrade the performance of the structure in any measurable way. Figure 76 shows that a significant void content was present in the first few composite structures produced. The cure process was subsequently modified to include several intermediate "debulking" steps. The intermediate debulking steps served to reduce void content to near-zero levels, as evidenced by the optical micrograph shown in Figure 77. The fibers are completely surrounded by the resin as verified by the polishing marks in the regions between the fibers.

[23] Mr. Russ Crutcher of MicroLab Northwest, 7609 140th Pl NE, Redmond, WA

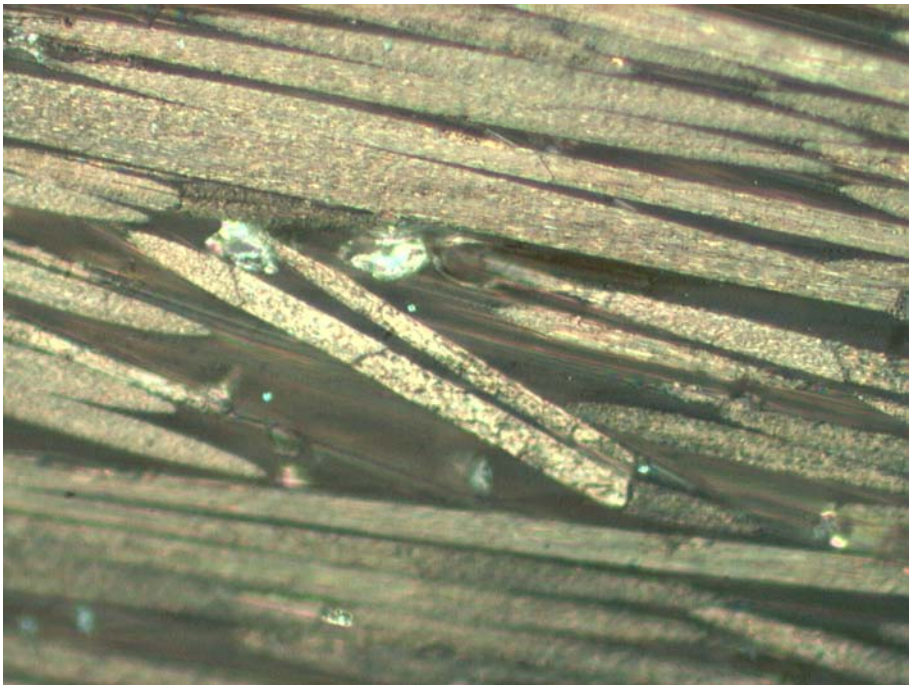


Figure 75 - Fractures found in the castellated outer shell (500X magnification).

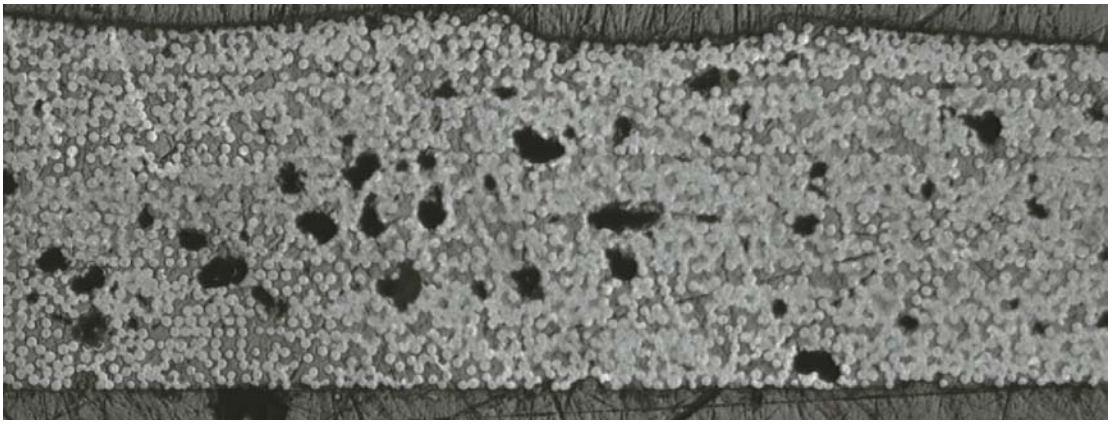


Figure 76. Voids present in a castellated outer shell without debulking (50X magnification).

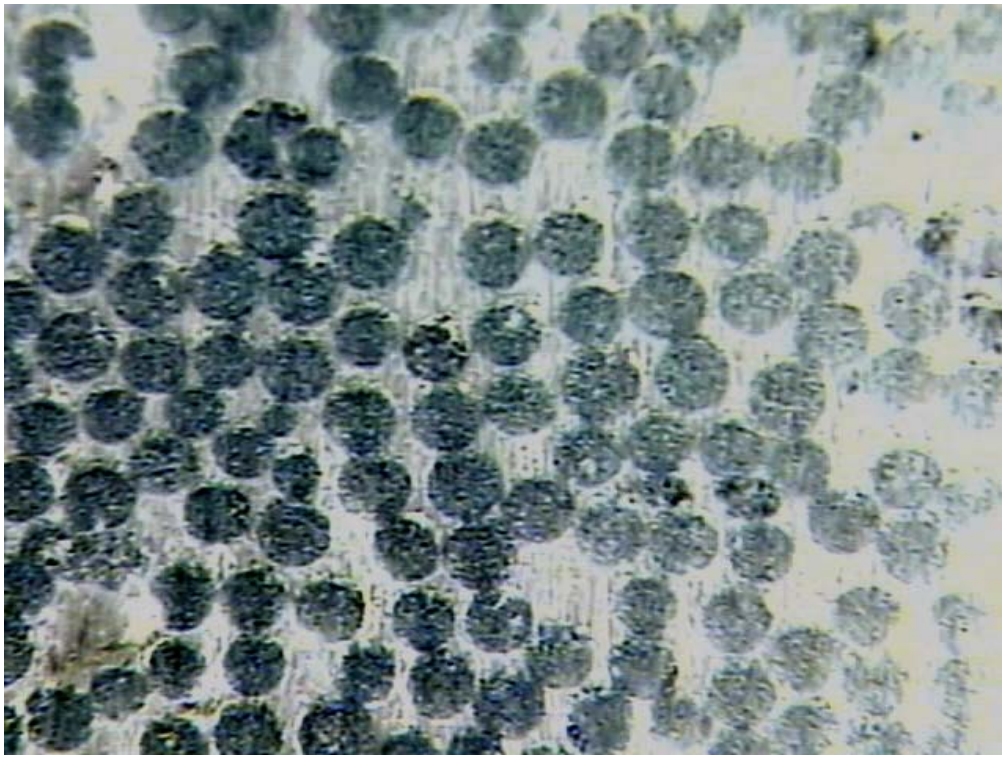


Figure 77. Void-free castellated outer shell produced using debulking steps during lay-up (1000X magnification).

4.3.5.2 Fabrication of Cooling System Components

The L0-1 cooling systems are assembled from a variety of components such as coolant tubes, bulkheads, manifolds, and support/cooling fins. An exploded view of the cooling system components for the L0b hybrids is shown below in Figure 78.

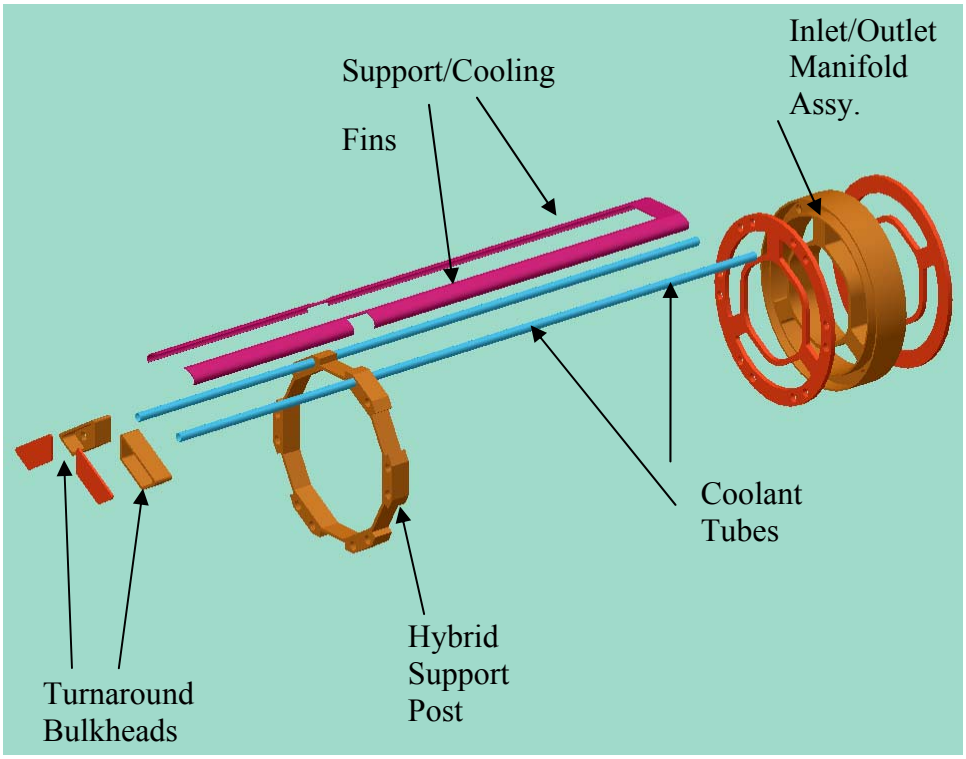


Figure 78. L0b hybrid cooling components

The fabrication methods used to produce the various components are as follows:

The coolant tubes are fabricated from K1392U/EX1515 carbon fiber pre-preg using techniques developed for the stave tubes at Lab 3. The material is wrapped around a soft RTV inner mandrel and compressed into a precision steel mold during the cure. The 4-ply stacking sequence is $[25°/-25°]_s$.

The support/cooling fins are fabricated from K13C2U/EX1515 carbon fiber pre-preg. The material is laid up over a precision steel form and cured using the standard vacuum bag/autoclave technique. The 4-ply stacking sequence is $[0°/90°]_s$.

The bulkheads, manifolds, and support parts are generally thicker and more complex than the other components, and will be CNC machined from pre-molded, fiber-filled, cyanate ester plates.

4.3.6 Assembly Procedures

4.3.6.1 Support Structure Shell Assembly

The sensor placement surface positions must be controlled to very high precision. The radial flexibility that is inherent in the geometry of the castellated shells results in a small ‘range’ of possible radial dimensions. The radial dimensions become fixed once the castellated shells are coupled to the inner shells. In order to precisely fix the sensor placement surfaces at the specified positions, the outer shell is adhesively bonded to the inner shell using precision tooling. The sensor cooling tubes run inside the castellations and are adhesively bonded to both the outer and

inner shells. Therefore it becomes necessary to include the sensor cooling tubes in the shell assembly process. A cross-section of the assembled L0 inner/outer shell, including the sensor cooling tubes, is shown in Figure 79.

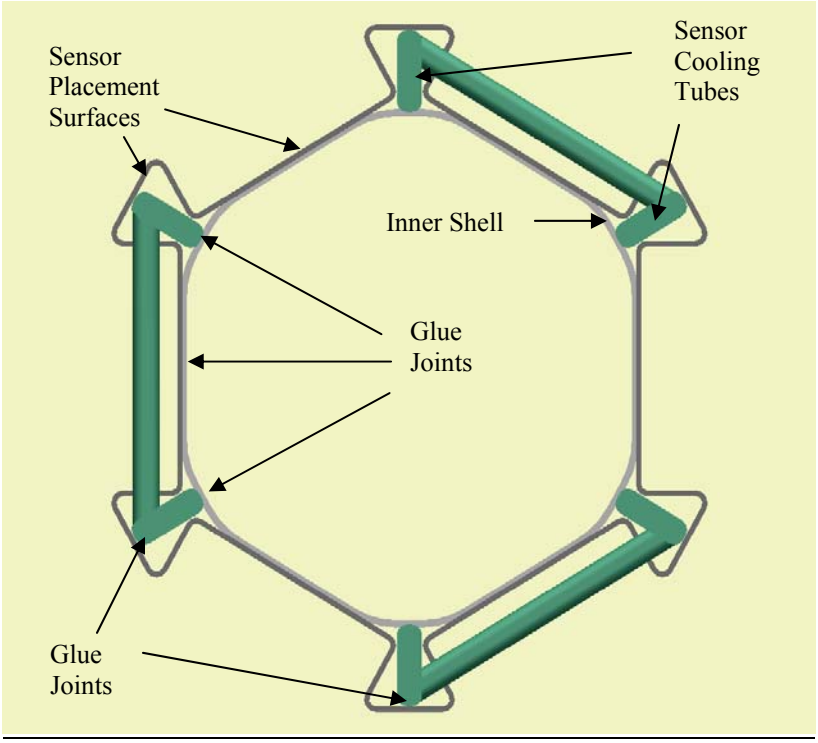


Figure 79. L0 support structure shell assembly

The shells will be joined using EX1516 cyanate ester B-staged film adhesive[24]. The cured film thickness is currently specified as 25 μm (.001"). A brief description of assembly procedures is discussed below.

The inner shell is slid onto the precision mandrel (Figure 80). Strips of film adhesive are then applied to the mating surfaces of the inner shell (the material has a light tack at room temperature).

[24] http://www.brytetech.com/adhesive.htm

Figure 80. L0 precision mandrel with inner shell

Strips of film adhesive are applied to the inner surfaces of the outer shell castellations where the cooling tubes are bonded. The outer shell and cooling tubes are then slid over the inner shell (Figure 81). The cooling tubes are not shown below – refer to Figure 26 of section 4.3.2.

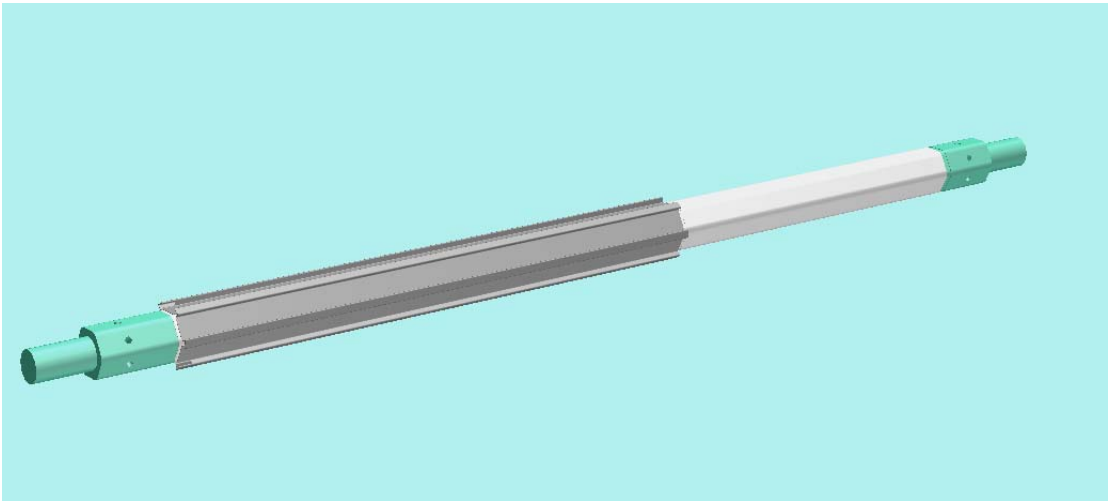


Figure 81. Outer shell installed over inner shell and cooling tubes (cooling tubes not shown).

Once the parts have been properly positioned a set of precision steel pressure-bars is installed onto the mandrel (Figure 82 and Figure 83). The bars have a step machined in the bottom that defines the overall distance between the mandrel surface and the outer surface of the castellated shell (Figure 84).

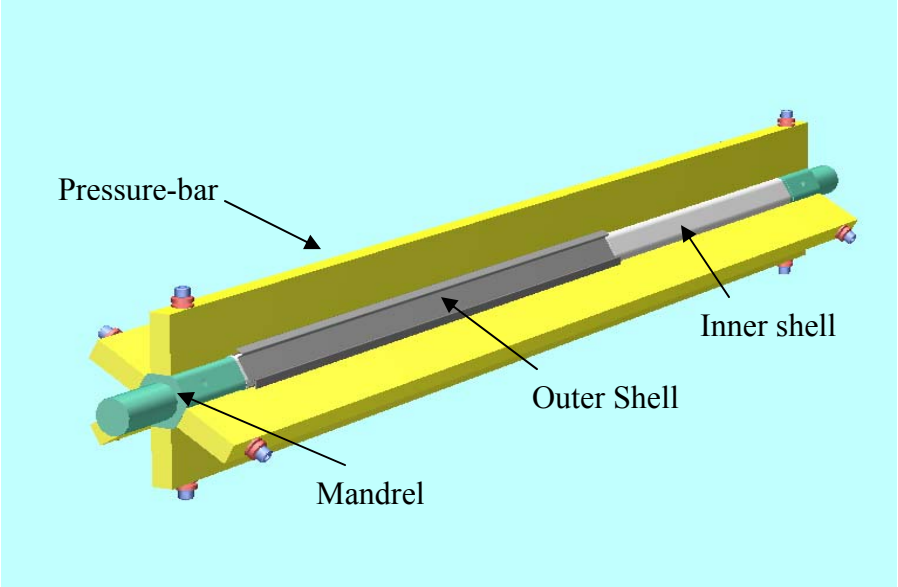


Figure 82. L0 shell assembly fixture

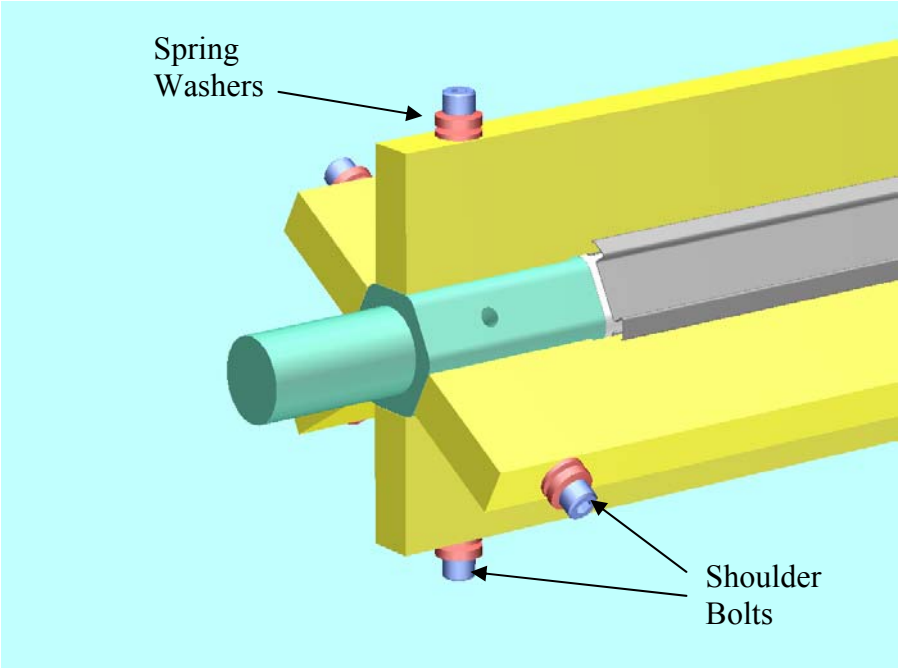


Figure 83. Detail of L0 shell assembly fixture

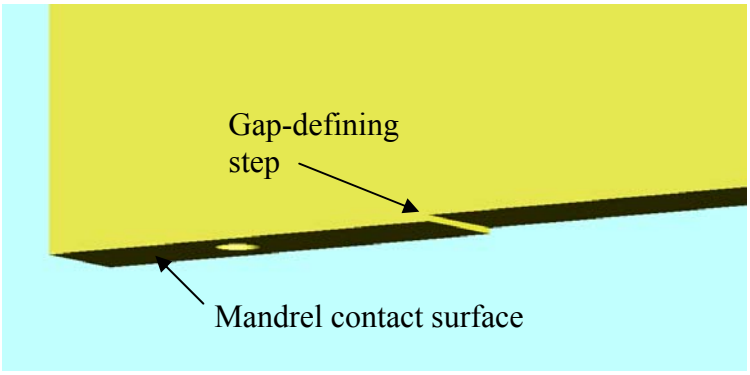


Figure 84. Pressure Bar

Shoulder bolts combined with spring washers are used to lightly clamp the bars to the mandrel (Figure 83). The entire assembly is placed into the oven in an upright position to avoid gravitational sag of the tooling. As the temperature ramps up, the film adhesive begins to soften and flow under the pressure of the tooling. At several intervals, the shoulder bolts are tightened to increase the pressure, until finally the bars are solidly stopped against the precision surfaces of the mandrel. The pressure-bar step dimension is chosen such that the adhesive film thickness is reduced by a pre-determined amount during the cure. Preliminary tests bonding Kapton film suggest an appropriate thickness reduction to be ~50% in order to insure a consistent, void free bond line. This infers a 50μm (.002") uncured film thickness – a readily available material size.

Quality Assurance

After the specified cure cycle has been completed, the shell assembly is taken to the CMM for dimensional surveying. An indexing fixture is used to hold and manipulate mandrels and parts during inspection. The index fixture and castellated mandrel are show below in Figure 85.

Figure 85. Index fixture with prototype mandrel

4.3.6.2 Cooling system assembly

The cooling tubes located inside the castellations in both L0 and L1 are incorporated in the basic structures of these layers during assembly of the shells as discussed above. The only remaining assembly needed for these parts of the cooling system is the connection of the tubes to the cooling manifolds.

L0 cooling system assembly

For L0 the complete cooling system (Figure 27) is pre-assembled on a jig. This includes the L0a hybrid supports and cooling tubes, the support bulkheads and the sensor cooling tubes with their turnaround bridges. All of these pieces are glued together with cyanate ester adhesive. The complete cooling system assembly can then be leak tested prior to final assembly of the castellated shell and the inner shell as described above. The L0b cooling system (Figure 31) is separately pre-assembled on a jig and leak tested prior to installation.

L0 final assembly

Final assembly of L0 will be done at FNAL on precision tooling. With the completed base structure and L0a hybrid cooling system installed on the tooling, the sensors and hybrids are installed in the following order:

1. Each sensor is connected by its analog cable to its hybrid and brought to the assembly site.
2. For each row of L0a, start with the sensor furthest from the IP.
3. Add the other five sensors, working progressively closer to the IP. Note that, as each hybrid is added, it goes over the analog cable of the previously installed hybrid. Special tooling is used to hold the cable down so that it does not push up on the hybrid as the glue cures. This is particularly important for the final hybrid as the space below it is now filled with five analog cables.
4. Repeat the above steps for the other five rows of sensors.

The L0b hybrid cooling assembly can now be slid over the assembly and fixed in position (Figure 33). The L0b sensors and hybrids are now installed in the same manner as the L0a ones.

L1 cooling assembly

For L1, the hybrid cooling manifold/bulkhead is pre-assembled on a jig and leak tested. The base assembly of the castellated shell, the inner tube, manifold/bulkhead and extension tube is then completed as discussed above and installed on the final installation tooling. The sensor/hybrid modules are then positioned precisely and glued in place.

4.3.7 Radiation Length Calculations

The average radiation lengths seen by particles traversing the L0 and L1 detectors have been estimated for the design described above and are summarized in Table 13 through Table 15. Table 13 and Table 14 give values in the silicon sensor region (- 480 mm < z < 480 mm) for L0 and L1, respectively. Table 15 gives the values in the region outside the active volume where the

L0 hybrids reside (500 mm < |z| < 800 mm). In all cases material of discrete objects such as hybrids is averaged over φ and along the beam direction. The amount of material in the hybrid circuits averaged over the area of the hybrid is estimated to be equivalent to 2.3%. Other radiation lengths are based on estimates of composition of the material. The details are included in the Tables.

For L0 in the silicon sensor region, the average material amounts to 1.51% of a radiation length of which about two thirds is due to silicon sensors and the mechanical support. The actual fractional contributions are: silicon 38%, analog cables and HV insulation 22%, cooling 14% and mechanical support 26%. The average material in the silicon sensor region for L1 is 2.93% of a radiation length of which the fractional contributions are: silicon 15%, hybrid circuits, digital cables and HV insulation 55%, cooling 10% and mechanical supports 20%. For the L0 hybrid region, the total material is 5.98% of a radiation length, of which about 60% comes from the hybrids and digital cables.

Table 13. L0 tracking volume radiation length calculations

Average material radiation length in L0 tracking volume	Material type	Object radiation length X_0	Object Length	Object width	Object thickness	Phi spread correction	Z spread correction	Average over surface	Subtotal	Fraction of Total
Central region (-480 < Z <480 mm)		mm	mm	mm	(mm)			% of X_0	% of X_0	%
Silicon									0.58	38.1%
L0A silicon sensor at r = 18.5 mm	Si	94.0	80.0	15.5	0.320	0.85	1.00	0.288		19.0%
L0B silicon sensor at r = 24.5 mm	Si	94.0	80.0	15.5	0.320	0.62	1.00	0.210		13.9%
Expoy layer under L0A (0.05 mm)	Epoxy	350.0	80.0	16.4	0.050	0.90	1.00	0.013		0.8%
Expoy layer under L0B (0.05 mm)	Epoxy	350.0	80.0	7.0	0.050	0.58	1.00	0.008		0.5%
HV pad for L0A and L0B	Varias	100.0	8.0	12.0	0.500	1.15	0.10	0.057		3.8%
Analog cables									0.27	18.0%
L0A analog cable 0.05 mm kapton 6 layers (at sensor #3/4 boundary)	Kapton	284.0	80.0	14.0	0.300	0.67	1.00	0.071		4.7%
L0A spacer mesh (10% kapton density)	Kapton	2840.0	80.0	14.0	1.500	0.67	1.00	0.035		2.3%
L0A analog cable copper (6 layers, 0.01x0.005 mm trace)	Cu	14.0	80.0	2.8	0.030	0.13	1.00	0.029		1.9%
L0A analog cable 1 micron gold plating	Gold	3.0	80.0	2.8	0.006	0.13	1.00	0.027		1.8%
L0B analog cable Kapton	Kapton	284.0	80.0	14.0	0.300	0.51	1.00	0.054		3.6%
L0B analog cable copper	Cu	14.3	80.0	2.8	0.030	0.10	1.00	0.022		1.4%
L0B analog cable gold	Gold	3.0	80.0	2.8	0.006	0.10	1.00	0.021		1.4%
Cable strain relief	BeO	133.0	5.0	15.0	0.254	0.55	0.06	0.007		0.4%
Wire bond protection	BeO	133.0	1.5	15.0	1.000	0.55	0.02	0.008		0.5%
HV insulation									0.05	3.6%
Castellated Kapton shell (2 x 25 micron)	Kapton	284.0	80.0	17.0	0.050	1.71	1.00	0.030		2.0%
Epoxy (2x25 micron)	Epoxy	350.0	80.0	17.0	0.050	1.71	1.00	0.024		1.6%
Cooling									0.22	14.5%
CF tubing (2x5 mm, 0.3 mm wall)	CF/epoxy	250.0	80.0	14.0	0.300	0.67	1.00	0.080		5.3%
Coolant	40% EG	358.0	80.0	2.0	5.000	0.10	1.00	0.133		8.8%
Epoxy for gluing cooling tube	Epoxy	250.0	80.0	3.0	0.100	0.12	1.00	0.005		0.3%
Mechanical support									0.39	25.8%
Inner shell 0.2 mm thick at <r> = 17mm	CF/epoxy	250.0	80.0	8.9	0.200	1.00	1.00	0.080		5.3%
Castellated shell 0.40 mm thick	CF/epoxy	250.0	80.0	17.0	0.400	1.71	1.00	0.273		18.1%
Epoxy between two shells (0.10 mm)	Epoxy	250.0	80.0	16.0	0.100	0.87	1.00	0.035		2.3%
Al ground strips 0.025 mm10% surface	Al	89.0	80.0	2.0	0.025	0.11	1.00	0.003		0.2%
							Total	$\%X_0$ =	1.51	100.0%

Table 14. L1 tracking volume radiation length calculations

Average material radiation length in L1 tracking volume	Material type	Object radiation length X_0	Object Length	Object width	Object thickness	Phi spread correction	Z spread correction	Average over surface	Subtotal	Fraction of Total
Central region (-480 < Z <480 mm)		mm	mm	mm	(mm)			% of X_0	% of X_0	%
Silicon									0.45	15.5%
L1A silicon sensor at r = 35.0 mm	Si	94.0	80.0	25.0	0.320	0.68	1.00	0.232		7.9%
Expoy layer under L1A (0.05 mm)	Epoxy	350.0	80.0	25.0	0.050	0.68	1.00	0.010		0.3%
L1B silicon sensor at r = 39.2 mm	Si	94.0	80.0	25.0	0.320	0.60	1.00	0.203		6.9%
Expoy layer under L1B (0.05 mm)	Epoxy	350.0	80.0	25.0	0.050	0.60	1.00	0.009		0.3%
Hybrid+digital cable									1.57	53.5%
L1A hybrid (average = 2.3% r.l.)	Varies	43.5	22.5	25.0	1.000	0.68	0.28	0.441		15.0%
L1A digital cable 0.25 mm kapton	Kapton	284.0	80.0	14.8	0.250	0.38	1.50	0.050		1.7%
L1A digital cable 2x0.05 mm Al shielding	Al	89.0	80.0	14.8	0.100	0.38	1.50	0.064		2.2%
L1A digital copper 0.0079g/cm^2	Cu	14.3	80.0	11.1	0.090	0.29	1.50	0.271		9.2%
L1B hybrid (average = 2.3% r.l.)	Varies	43.5	22.5	25.0	1.000	0.60	0.28	0.386		13.2%
L1B digital cable 0.25 mm kapton	Kapton	284.0	80.0	14.0	0.250	0.33	1.50	0.044		1.5%
L1B digital cable 0.05 mm aluminum	Al	89.0	80.0	14.0	0.100	0.33	1.50	0.056		1.9%
L1B digital copper, 0.0079g/cm^2	Cu	14.0	80.0	11.1	0.090	0.27	1.50	0.256		8.7%
HV insulation									0.04	1.3%
Castellated Kapton shell (2 x 25 micron)	Kapton	284.0	80.0	22.0	0.050	1.2	1.00	0.021		0.7%
Epoxy (2x25 micron)	Epoxy	350.0	80.0	22.0	0.050	1.17	1.00	0.017		0.6%
Cooling									0.29	9.8%
CF tubing 2x(5+2.6) mmx0.3 mm wall	CF/epoxy	250.0	80.0	30.4	0.300	0.78	1.00	0.094		3.2%
Epoxy for gluing cooling tubes	Epoxy	350.0	80.0	30.4	0.050	0.78	1.00	0.011		0.4%
Coolant	40% EG	358.0	80.0	4.9	2.630	0.25	1.00	0.182		6.2%
Mechanical support									0.39	13.2%
Inner shell 0.4 mm thick at <r> = 34 mm	CF/epoxy	250.0	80.0	17.8	0.400	1.00	1.00	0.160		5.5%
Pyrolistic graphite sheet at <r> = 34 mm	Carbon	438.0	80.0	17.8	0.100	1.00	1.00	0.023		0.8%
Castellated shell 0.40 mm thick	CF/epoxy	250.0	80.0	22.0	0.400	1.19	1.00	0.190		6.5%
Epoxy strips between inner/outer shells	Epoxy	250.0	80.0	25.0	0.050	0.70	1.00	0.014		0.5%
Electric ground strips 10% surface	Al	89.0	80.0	3.0	0.013	0.09	1.00	0.001		0.0%
L1 outer shell									0.20	6.8%
L1 outer shell at r = 45 mm	CF	250.0	80.0	20.0	0.500	1.00	1.00	0.200		6.8%
							Total	$\%X_0$ =	2.93	100.0%

Table 15. L0 hybrid region radiation length calculation

Average material radiation length in L0 hybrid region End region (500 < |Z| <800 mm)	Material type	Object radiation length X_0 mm	Object Length mm	Object width mm	Object thickness (mm)	Phi spread correction	Z spread correction	Average over surface % of X_0	Subtotal % of X_0	Fraction of Total %
L0 hybrid+digital cables									3.62	60.5%
L0A hybrid (average = 2.3% r.l.)	Varies	43.5	37.0	18.0	1.000	0.75	0.88	1.514		25.3%
L0A digital cable, 0.25 mm kapton	Kapton	284.0	42.0	14.8	0.250	0.54	2.50	0.120		2.0%
L0A digital cable 2x0.05 mm Al shielding	Al	89.0	42.0	14.8	0.100	0.54	1.50	0.092		1.5%
L0A digital cable 0.0079g/cm^2 copper	Cu	14.3	42.0	11.1	0.090	0.41	1.50	0.385		6.4%
L0B hybrid (average = 2.3% r.l.)	Varies	43.5	42.0	18.0	1.000	0.49	1.00	1.130		18.9%
L0B digital cable 0.25 mm kapton	Kapton	284.0	42.0	14.0	0.250	0.35	1.50	0.046		0.8%
L0B digital cable 0.05 mm aluminum	Al	89.0	42.0	14.0	0.100	0.35	1.50	0.059		1.0%
L0B digital copper 0.0079g/cm2	Cu	14.0	42.0	11.1	0.090	0.28	1.50	0.269		4.5%
Analog cable									0.26	4.3%
L0A analog cable 0.05 mm kapton 6 layers (at hybrid #3/4 boundary)	Kapton	284.0	42.0	14.0	0.300	0.67	1.00	0.071		1.2%
L0A spacer mesh (10% kapton density)	Kapton	2840.0	42.0	14.0	1.500	0.67	1.00	0.035		0.6%
L0A analog cable copper (6 layers, 0.01x0.005 mm trace	Cu	14.0	42.0	2.8	0.030	0.13	1.00	0.029		0.5%
L0A analog cable 1 micron gold plating	Gold	3.0	42.0	2.8	0.006	0.13	1.00	0.027		0.4%
L0B analog cable Kapton	Kapton	284.0	42.0	14.0	0.300	0.41	1.00	0.043		0.7%
L0B spacer mesh (10% kapton density)	Kapton	2840.0	42.0	14.0	1.500	0.39	1.00	0.021		0.3%
L0B analog cable copper	Cu	14.3	42.0	2.8	0.030	0.08	1.00	0.017		0.3%
L0B analog cable 1 micron gold plating	Gold	3.0	42.0	2.8	0.006	0.08	1.00	0.016		0.3%
L0 Cooling tube and coolant									0.69	11.6%
L0 sensor CF tubing (6)	CF/epoxy	250.0	42.0	14.0	0.300	0.67	1.00	0.080		1.3%
L0 sensor coolant	40% EG	358.0	80.0	2.0	5.000	0.10	1.00	0.133		2.2%
L0A hybrid CF tubing (12) 3.3 mm OD	CF/epoxy	250.0	42.0	9.4	0.300	0.67	1.00	0.080		1.3%
Epoxy for gluing cooling tubes	Epoxy	350.0	42.0	10.4	0.050	0.27	1.00	0.004		0.1%
L0A hybrid coolant	40% EG	358.0	42.0	9.4	0.750	0.67	1.00	0.073		1.2%
L0A hybrid cooling tube support	CF/epoxy	250.0	42.0	10.0	0.500	0.76	1.00	0.080		1.3%
L0B hybrid CF tubing (12) 3.3 mm OD	CF/epoxy	250.0	42.0	9.4	0.500	0.56	1.00	0.113		1.9%
Epoxy for gluing cooling tubes	Epoxy	350.0	42.0	10.4	0.050	0.27	1.00	0.004		0.1%
L0B hybrid coolant	40% EG	358.0	42.0	9.4	0.750	0.56	1.00	0.062		1.0%
L0B hybrid cooling tube support	CF/epoxy	250.0	42.0	10.0	0.500	0.60	1.00	0.063		1.0%
L0 shells and bulkheads									0.58	9.7%
L0 Inner shell 0.5 mm thick <r> = 17 mm	CF/epoxy	250.0	42.0	8.9	0.500	1.00	1.00	0.200		3.3%
L0 outer shell 0.5 mm thick <r> = 40 mm	CF/epoxy	250.0	42.0	20.9	0.500	1.00	1.00	0.200		3.3%
Three bulkheads (10x8 mm ring)	Byrilium	303.4	24.0	15.7	8.000	1.00	0.07	0.181		3.0%
L1 items									0.83	13.9%
12 CF tubing 2x(5+2.6) mm 0.3 mm wall	CF/epoxy	250.0	42.0	15.2	0.300	0.68	1.00	0.081		1.4%
Sensor/hybrid A32Coolant	40% EG	358.0	42.0	4.9	2.630	0.22	1.00	0.084		1.4%
Digital cable 0.25 mm kapton	Kapton	284.0	42.0	14.0	0.250	0.31	1.00	0.027		0.5%
Digital cable 0.05 mm aluminum shielding	Al	89.0	42.0	14.0	0.100	0.31	1.00	0.035		0.6%
Digital cable 0.0079g/cm^2 copper	Cu	14.0	42.0	10.5	0.090	0.23	1.00	0.150		2.5%
L1 inner shell at r = 40 mm	CF/epoxy	250.0	37.0	23.6	0.500	1.00	1.00	0.211		3.5%
L1 outer shell at r = 45 mm	CF/epoxy	250.0	42.0	23.6	0.500	1.00	1.00	0.240		4.0%
							Total	$\%X_0$ =	5.98	100.0%

4.4 Layer 2-5 Mechanical Design

The outer four layers of the tracker consist of 168 staves, 84 in each sub-barrel. Each stave contains four silicon modules, two axial and two small angle stereo. The stave provides active cooling to remove the heat generated by the readout electronics and the sensors, maintains the planarity of the silicon sensors, and provides for the accurate alignment of the sensor planes in space.

4.4.1 Readout configuration

The azimuthal multiplicity of each sensor layer must be divisible by 6 in order to fit in the existing silicon track trigger. Although not a hard constraint, we felt it very desirable to limit the number of sensor and hybrid types, our goal being only one sensor type for all four outer layers. This leads to ϕ segmentation of 12, 18, 24 and 30 in layers 2, 3, 4 and 5, respectively. Given the radii of these layers ($\approx$50-160mm) the necessary sensor active width is determined to be 32-38mm. We wish to produce two sensors per 6" silicon wafer, so the length of the sensors is limited to ~110mm. To obtain the desired η coverage, layers 2-5 should have 600mm of sensor coverage (each side of z=0). This leads to a natural choice of 100mm for the sensor length.

The readout cable plant is limited to about 912 by the existing electronics. Of these, 216 are reserved for the inner two layers of the tracker. Dead time considerations limit the total number of SVX channels that can be accommodated on one readout cable; this limit is 10 chips for layers 2-5. The available cable plant cannot accommodate fine pitch (50-60 μm) readout with fine (100 mm) z-segmentation. Simulations of resolutions, pattern recognition and occupancy found a substantial preference for finer pitch over finer z segmentation. In addition, finer pitch also allows for direct wire bonding from the SVX chips to the sensors. We have chosen a sensor design with 639-channels at 60 μm pitch, for an active width of 38.4 mm.

Figure 86: Readout configuration for outer layer staves. The axial modules are shown above and the stereo modules below.

The outer layers (layers 2-5) contain staves six sensors long (Figure 86). The hybrid-sensor modules closest to z=0 within a stave are 200 mm long and have two 100 mm readout segments. Those further from z = 0 are 400 mm long and have two 200 mm readout segments. To form the

200 mm readout segments, two 100 mm sensors are glued end-to-end and electrically coupled with wirebonds on the top surface and a bias connection between the back planes.

4.4.2 Silicon modules

The outer layer silicon modules consist of two or four silicon sensors, each 100 mm in length by 40.34 mm in width, joined together with a single readout hybrid. The readout hybrid is double-ended, meaning that the hybrid straddles two sensors with separate SVX chips reading out the signals from each end. There are four types of modules labeled by the length in centimeters of the sensor segment read out and whether their sensors are aligned axially or with a stereo angle. The same sensors are used in all four of the module types. There are two hybrid types, one for the axial modules and one for the stereo modules. The two axial modules differ only in the number of sensors used, while the two stereo module types use different stereo angles depending on the lengths of the readout segments; 1.24 degrees for 200mm readout, 2.48 degrees for 100mm readout. While the larger stereo angle would be preferred throughout the device, tight geometrical constraints limit the width of the staves, and hence the maximum allowable stereo angle as a function of readout length.

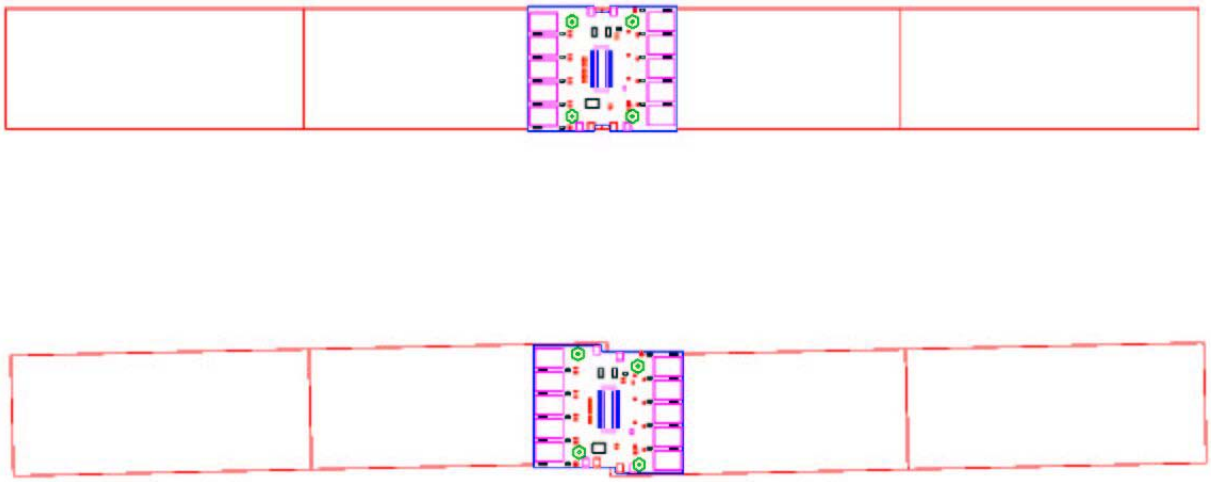


Figure 87: Module assemblies. Top: A 20-20 axial module. Bottom: A 20-20 stereo module.

Each hybrid has 10 SVX chips, 5 at each end of their 50mm length. Each SVX chip generates 0.3-0.5W of heat, with 50% of that heat load concentrated in narrow regions near the two ends of the chip. For design purposes we have assumed a 0.5W load per chip. A connector located at the center of the hybrid provides the power, control signals for the chips and the high voltage for the sensor bias. A bias line wraps around the edge of the sensor to provide a connection directly to the back plane of the sensor. Ground connections also wrap around the edge of the sensor-hybrid modules to tie the conductive support structure to the local hybrid ground in order to minimize ground current and pickup effects.

The techniques for assembly of sensor modules are similar to those used in the past by many groups, including DØ. Sensors are manually aligned with optical feedback from a camera mounted on a coordinate measurement machine (CMM). Once aligned, the sensors are glued to

one another, directly or via a connecting substrate. Reasonable expectations for this alignment are a few microns. The hybrid, previously assembled, burned-in and tested, is glued directly to the silicon sensors. Wire bonding is then done between the hybrid and the sensors, and from sensor to sensor for the modules with 200mm readout segments. The sensor pitch has been chosen so that the hybrid to sensor bonding can be done directly from the SVX chips to silicon sensors without a pitch adapter. The total numbers of wire bonds required for layers 2-5 are 430K sensor-to-sensor plus 860K hybrid-to-sensor, for a total of 1290K bonds. For the longer modules, the sensor-to-sensor wire bonding can be done either before or after the hybrid is mounted. Sensor alignment and sensor-to-sensor wire bonding can proceed prior to hybrid delivery, should that become a production constraint.

Prior to assembly into staves the completed module will undergo electrical testing, additional burn-in and in some cases laser scanning (described elsewhere in this document).

4.4.3 Stave assemblies

The outer four layers of the silicon tracker are constructed as 168 staves, approximately 46mm wide by 8.9mm tall by 610mm in length (Figure 88). Each stave is independently mounted to a set of bulkheads, described previously. The stave structures consist of a core with silicon mounted to both surfaces and two external C-channels that stiffen the structure. The core structure has an integrated cooling circuit to remove the heat generated by both the hybrid electronics and the silicon sensors. The core also provides the precise reference features for aligning and mounting sensor modules to the core and the completed stave to the bulkheads. Finally, the core maintains the flatness of the silicon sensors. The external C-channels provide the necessary bending and torsional stiffness to the stave.

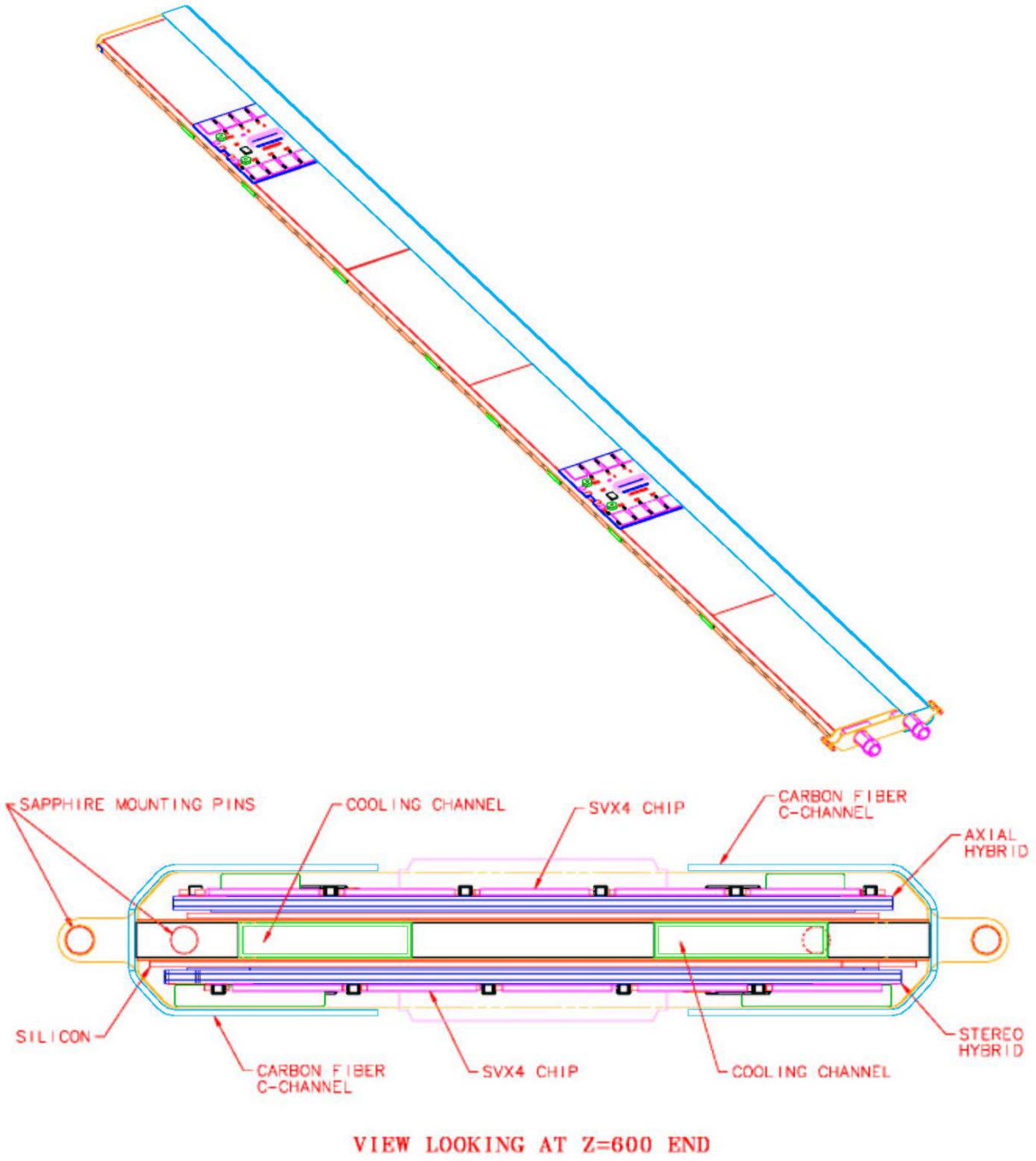


Figure 88: Stave assembly drawings. The upper drawing shows a isometric view of the stave with one of the C-channels removed. The lower plot is an end view of a complete stave assembly.

The core structure is about 2mm tall. The main element is the cooling tube. The tube is made from high strength carbon fiber (IM7 or similar) with a cyanate ester resin (Bryte EX-1515 or similar) that features very low moisture absorption. The cooling passage is 2mm tall by 10mm wide (outside) with a 200-250 micron wall thickness. The tube is a U-shape, turning around near Z=0. The mechanical structure is built up from this tube using "outriggers" made of similar tube to carry the silicon module load out to the C-channels. The remaining space will likely be filled with Rohacell foam to provide a uniform mounting surface for the sensors. The core structure will be laminated with 50 micron Kapton MT, a polyimide loaded with alumina for better thermal conductivity, to provide an electrically insulating layer between the back plane of the sensors, at 300V, and the tube, which will be grounded. The fluid dynamics, thermal performance and mechanical performance of this structure are described below. Precision mounting and alignment features - ruby and sapphire rods and spheres - are an integral part of the core structure. Once assembled, the core structure can be leak checked and inspected for dimensional tolerances prior to population with silicon modules.

The silicon modules are bonded directly to the stave core. One side of the core is populated with axial sensor modules while the other is populated with small angle stereo modules. The mounting and reference features on the stave core are accessible from both sides of the stave so that they can be used to establish the reference system on a CMM for alignment of the silicon modules to the stave core. Past experience is that module-to-module alignment can be done at the sub-5μ level.

Carbon fiber C-channel structures mount to the core on each side with cross-members at several locations along the length of the stave. These structures provide most of the stiffness of the completed stave, provide a surface for the readout cables to attach to as they run to the end of the stave, and help to protect the sensors and hybrids from damage during further processing steps.

4.4.4 Stave mass and radiation length

The stave mass and radiation length have been estimated. The stave weight per unit length is 2.38g/cm. The radiation length (Table 16), averaged over the silicon area, is 2.53%X_0 per layer. The breakdown of the material is 0.68%X_0 sensors, 0.55%X_0 hybrids, 0.56%X_0 readout cables, 0.31%X_0 coolant and tube, and 0.43%X_0 for the stave structure and adhesives. The equivalent of 1.5 readout cables are included in this estimate; the first cable begins at Z=100mm and the second at Z=400mm. A track passing at normal incidence through the hybrids sees roughly 5.3%X_0 per layer. Near Z=0, where there are no cables or hybrids, the radiation length is only 1.4%X_0 per layer.

Table 16 - Breakdown of stave radiation length by material. The table below is for the layer 4-5 staves.

Item	Material	X0 (cm)	L (mm)	W (mm)	t (mm)	%X0 (local)	%X0 (avg.)	Fraction
Silicon Sensor	Si	9.4	600.0	40.3	0.640	0.681	0.681	**26.9%**
SVX4 chips (5x2)	Si	9.4	36.0	32.0	0.720	0.766	0.036	
Epoxy (loaded, 50 micror	Loaded epoxy	10.0	36.0	32.0	0.100	0.100	0.005	
BeO substrate	BeO	13.3	100.0	38.4	0.760	0.571	0.091	
Dielectric layers	glass	12.7	100.0	38.4	0.720	0.567	0.090	
Metal Layers	Au	0.3	100.0	38.4	0.029	0.960	0.152	
Surface Mount comps.	High Z	1.0	37.6	11.0	0.500	5.000	0.085	
Solder	Pb/Sn	0.9	26.2	38.4	0.200	2.222	0.092	**21.8%**
CF tube (2 x 10mm x 2mr	CF	25.0	600.0	20.0	0.575	0.230	0.114	
Coolant	40% EG	35.8	600.0	19.0	1.500	0.419	0.197	**12.3%**
Skins (Kapton MT)	Kapton	28.4	600.0	46.2	0.100	0.035	0.040	
Rohacell 51 foam spacer	Rohacell 51	806.0	600.0	26.2	1.778	0.022	0.014	
Pins	Sapphire	7.3	18.0	1.6	1.245	1.705	0.002	
Pin holders (G-10 and CF	G-10	19.4	18.0	16.0	1.900	0.979	0.012	
Epoxy (structural)	Epoxy	35.0	600.0	46.2	0.150	0.043	0.049	**4.6%**
C-channels	CF	25.0	600.0	36.0	0.760	0.304	0.271	
Epoxy (structural)	Epoxy	35.0	600.0	3.0	0.500	0.143	0.011	**12.0%**
Readout cables Kapton	Kapton	28.4	600.0	14.9	0.467	0.164	0.061	
Readout cable copper	Cu	1.4	600.0	11.9	0.235	1.680	0.496	**22.0%**
Total							**2.531**	**100.0%**

4.4.5 Stave mechanical connection

The staves are mounted to a pair of bulkheads, located at Z=0 and Z=600mm, that are coupled to each other by carbon fiber cylinders. The carbon fiber cylinders have a coefficient of thermal expansion (CTE) very near zero, while the staves are expected to shrink by roughly 6μ between assembly at room temperature and operation with –14C coolant (see Figure 90 in the section on stave thermal performance). In addition there may be some relative motion of the bulkheads, particularly longitudinally, during transportation and installation of the device. In the transverse direction the spacing between the mount points is ~50mm so the differential contraction of the stave and carbon fiber bulkheads is only expected to be 2-3μ. This is negligible and need not be considered in the mount design. Were the bulkheads fabricated in beryllium rather than carbon fiber this differential contraction would be 15μ and the mounts would need to be redesigned to allow for this.

In order to allow for longitudinal motion we intend to use mounts consisting of sapphire rods inserted into ruby orifices. These parts are commercially available with a tolerance range of ±5μ on the fit. The stave will have two pins located at the outer end that engage the outer bulkhead at either side of the stave along the stave mid-plane, and similarly at the Z=0 end two pins emerge from between the sensors to engage the Z=0 membrane. A longitudinal constraint will fix the Z=600mm end of the stave to the outer bulkhead, allowing the stave to retract from the Z=0

membrane during cool-down. A four-point mount is necessary since the staves do not have large torsional stiffness (θ/τ=1mrad/120g-mm) compared to their mass (140g) and width (40mm).

4.4.6 Alignment precision and stave mounts

The alignment requirements for the sensors are determined by the requirements of the impact parameter trigger. The trigger does not have the stereo sensor information so any misalignment of the axial sensors to the beam axis results in a degradation of the r-ϕ resolution at the trigger level. The intrinsic device resolution is $\approx 8\mu$.

The roll angle, i.e. rotation around an axis parallel to the beam line, does not affect trigger resolution, provided that it is known from survey. For a rotation in the plane of the sensors (yaw), the desired alignment tolerance is $<10\mu$ over a readout segment, or an angle of $<50\mu$rad. This results in an r.m.s. alignment tolerance of $\pm 30\mu$ over the full stave length. The pitch angle affects strips at the edges of the sensors, but not at the center. For a radial deviation dR at an angle ϕ from the center of the sensor, the transverse measurement error dX is given by $dX = dR\tan\phi$. The worst case is at the edges of the sensors where $\tan\phi = 0.27(0.11)$ in layer 2(5). This implies a radial positioning tolerance of $\pm 110(285)\mu$ over the length of a stave in layer 2(5). If the sensors are not held flat within the stave the effect is identical to that of the pitch angle. Here the length scale is 100mm, so the tolerance on the sensor flatness is of order 20μ. It is difficult to anticipate the degree of warping which the production sensors will have due to stresses induced in manufacturing. Very flat vacuum fixtures will be used to hold the sensors flat during bonding to the core. The 2mm tall core structure with sensors on both sides provides a significant moment of inertia to constrain the sensors flat.

The tolerances on the pins and orifices intended for mounting the staves are sufficiently tight to permit a mounting system without adjustment, provided the orifices can be located in the bulkheads with high precision. This is considered to be feasible.

4.4.7 Layer 2-5 stave thermal performance

The mechanical and thermal characteristics of the staves have been evaluated both analytically and using finite element analysis (FEA). The radiation environment of Run IIb affects both the depletion voltage and the leakage current (noise) of the silicon sensors. The former depends on the magnitude of the reverse annealing term, which saturates for temperatures below 0C and is fairly insignificant up to temperatures of +10C. Here the relevant temperature is the peak temperature on the sensors. The leakage current for a strip, and hence the associated noise, depends on the integrated current along the strip, and hence is a function of the average temperature, with appropriate weighting, along the strip. We have used the FEA temperature profiles to calculate the expected strip currents and then used this to extract an equivalent temperature, corresponding to the uniform temperature that would produce the same leakage current. Our design goal is <15% degradation in signal to noise ratio, with a minimum S/N of 10 at $20 fb^{-1}$. The result is that the equivalent temperature should be kept below 0C in layer 2 and below +5C in layers 3-5.

The stave cooling channel will operate below atmospheric pressure, hence the pressure drop is limited to ≈3psi. The total stave heat load is dominated by the hybrids that generate up to 20W, while the sensors are not expected to contribute more than 3W in layer 2 after $30fb^{-1}$ of exposure. The expected operating point for the stave is a flow rate of 0.175lpm resulting in a pressure drop of 2.6psi from inlet to outlet with a bulk temperature rise of 1.9C. The tube wall will operate roughly 7C above the bulk temperature locally under the hybrids.

Figure 89 shows the result of a finite element analysis (FEA) of the stave structure. This model assumes a heat transfer coefficient of $835W/m^2K$, as expected for the design flow, and an inlet fluid temperature of –14C. The maximum temperature on the structure is –1.0C on the hybrid, while the maximum temperature on the sensor is –4.3C. Experimental studies are underway to confirm the FEA results. Figure 90 shows the thermal distortions expected in the silicon sensors, perpendicular to the plane of the sensor and longitudinally. The thermal distortions are less than 10μ.

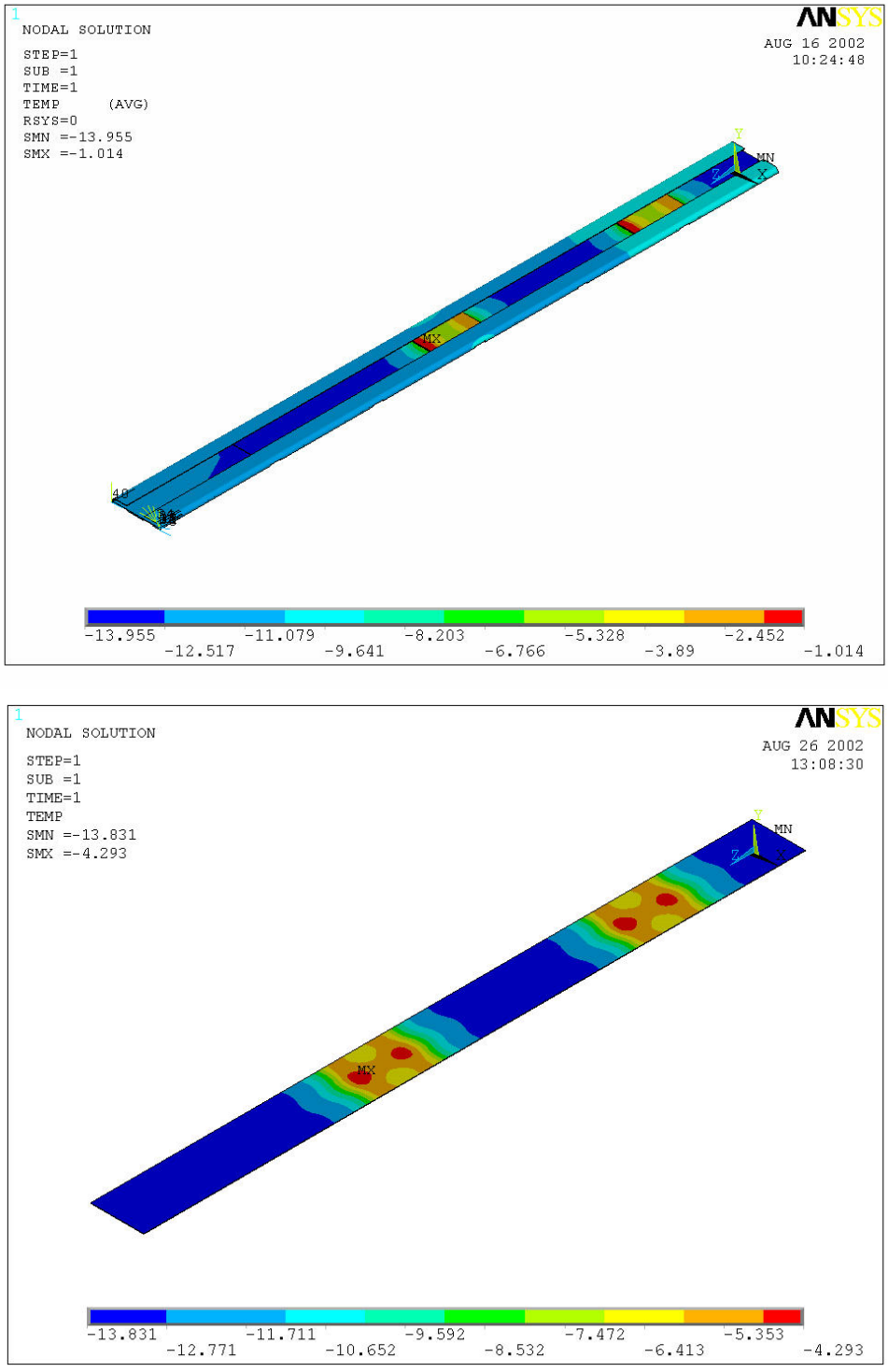


Figure 89: FEA results for the stave temperature profile. Coolant is assumed at -14C with a heat transfer coefficient of 835 W/m^2K. The upper plot shows the full stave structure, with the hottest region on the SVX chips, while the lower plot shows only the silicon sensor temperature profile.

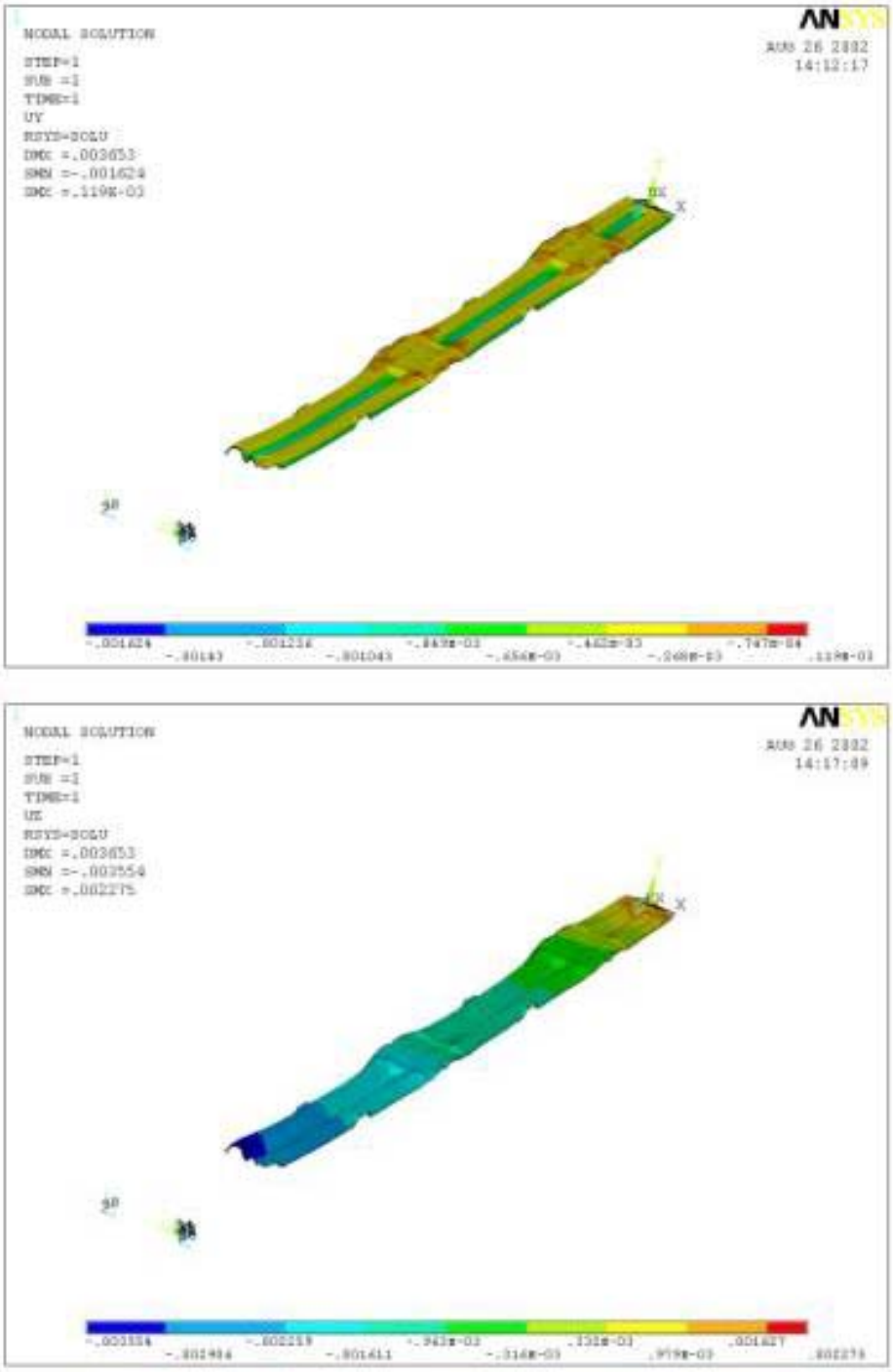


Figure 90: FEA results for the stave thermal distortion. Coolant temperature is –14C. Dimensions shown are in mm. The upper plot shows the displacement perpendicular to the sensor planes, the lower plot the displacement along the axis of the stave. Only the silicon is shown in the figures. Note that the object shown is ½ width, where a symmetry boundary condition is used along the centerline (far edge) of the stave.

4.4.8 Layer 2-5 stave mechanical performance

Mechanical performance of the stave has been evaluated using both analytical and FEA calculations, with good agreement between these results. The expected deflection of the staves is under 60μ with static gravitational loading (Figure 91). While somewhat larger deflections may not adversely affect the detector resolution, they lead to stave natural frequencies that are approaching the 60Hz range and the possible reduction in stave mass is negligible compared to the mass of the sensors, electronics and cables. In addition, reduced deflection allows for tighter installation and assembly clearances and easier handling during fabrication and installation of the staves into the barrel assemblies.

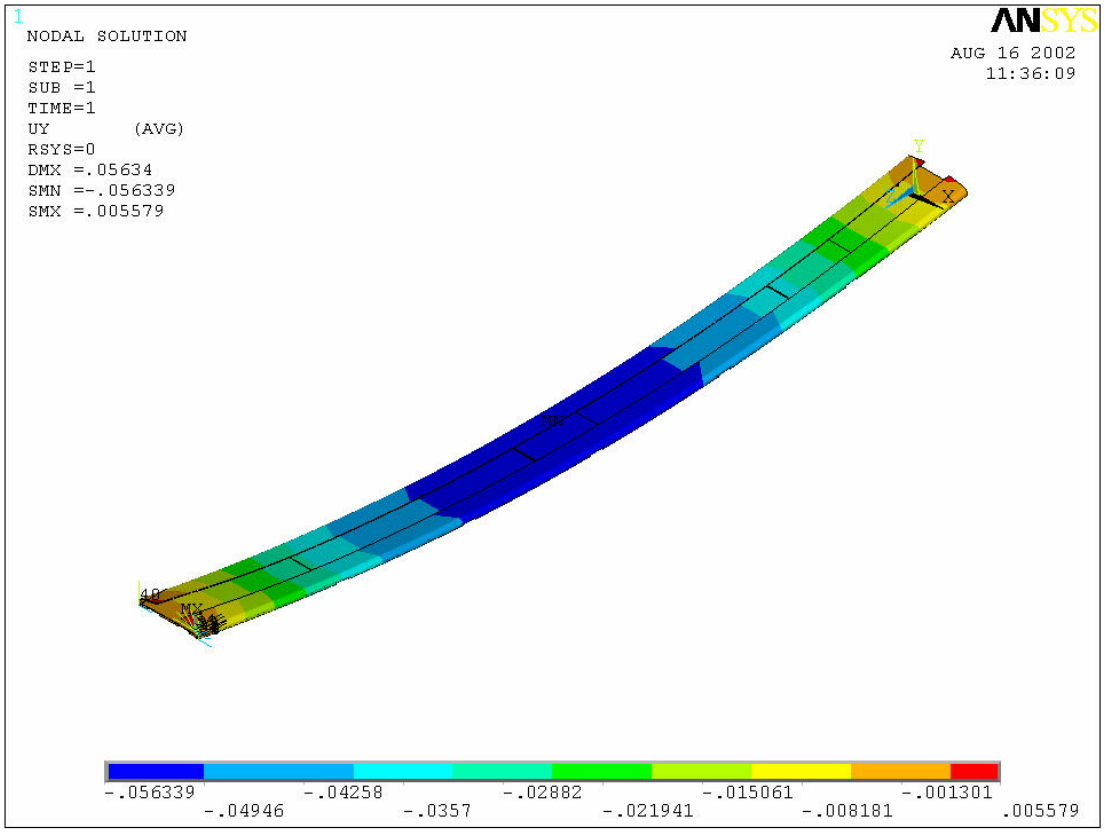


Figure 91: Stave deflection results for gravitational loading.

We have looked at extreme load conditions, for example application of a 1 kg load at the center of the stave, to study the robustness of the design. We find that, while the deflections are quite large, the stress levels in the sensors and structural elements remain far from failure levels. These studies were primarily aimed at understanding the handling requirements during fabrication and assembly.

A critical issue for the sensor alignment precision is deflection of the staves from external loads, in particular loads induced through the cables and cooling lines. To induce a 100μ deflection at

the center of the beam requires a moment of 35kg-mm (3.0in-lbs). This is well above what could be induced through the external connections to the staves.

4.5 Installation of the Run IIb Silicon Tracker

The Run IIb silicon tracker is to be delivered to the DØ experimental hall in two halves, north and south. We intend to deliver these halves in a manner similar to the one used for the Run IIa tracker. Unlike Run IIa, the two halves of the detector will be mated prior to installation into the central fiber tracker (CFT). This is necessary in order to achieve the required alignment. For Run IIa the two silicon barrel support structures were surveyed in the CFT on a CMM prior to installation of the CFT. The silicon was then aligned to the barrel support structures based on those surveys. This is not possible for the Run IIb device.

For Run IIa, each half of the detector was packaged in a protective enclosure prior to transportation. This enclosure provided mechanical protection of the assembly, storage for the cables attached to the assembly and a sealed gas volume that could be purged with nitrogen to prevent condensation and or contamination. The shipping enclosure also had an integrated rail system that was previously aligned to existing rails inside the CFT so that the detector halves could be slid directly into the CFT from the enclosure, one from each end. A set of roller bearings mounted from the enclosure provided a coupling to a trolley system used to move the silicon tracker inside the DØ detector cathedral and calorimeter gap areas. To reduce loads during transportation an air-ride cart was built which provided a stable rolling platform for each detector half. Once mounted inside the protective enclosure, each half of the detector was moved onto the cart. The cart was rolled to a loading bay, onto a truck lift gate and into the back of the truck. During several test runs and the final detector deliveries for Run IIa this cart consistently kept accelerations below 5g in all three directions. At DØ the cart was rolled back onto the lift gate and the detector was lifted off of the cart and delivered by crane to the assembly hall. At this point the detector was supported from above on roller bearings on a tube. This tube formed the first section of a trolley rail system used to bring the detector along the cathedral area into the calorimeter gap. When the detector arrived at the final turn into the CFT it was lowered onto a “table” mounted to the central calorimeter. Final alignment to the CFT was done by sliding the silicon tracker and enclosure base on the table surface.

For Run IIb we expect to use a similar enclosure for mechanical protection and dry gas purge. We will either reuse the existing air-ride cart or fabricate a similar one, for transporting the detector halves from the silicon detector facility to the DØ experimental hall. The detector is expected to remain on the beam line so it will not be possible to deliver the silicon tracker by crane directly from the truck to the detector cathedral area. Instead, the crane would be used to deliver the detector and cart to the floor of the assembly hall and the cart would then be rolled into the collision hall. A hoist would then be used to raise the silicon tracker up to the platform level. It may be possible to extend the trolley system used for the Run IIa installation to receive the Run IIb device directly from this hoist and deliver it to the calorimeter gap area. Both halves will be delivered to the same end of the CFT, mated and then slid into the CFT as one unit.

4.6 Alignment within the Fiber Tracker

The Level II silicon track trigger (L2STT)[25] of the DØ detector imposes limitations on the permissible magnitude of coherent misalignment of the Silicon Detector. The L2STT allows the selection of events that contain decays of long-lived particles by performing a precise reconstruction of charged particle tracks in the Silicon Detector and the CFT.

In addition to improving the resolution of the measurement of track p_T over that of the CFT alone (by a factor of 2-3 depending on p_T), the L2STT also determines the impact parameter of charged tracks with respect to the nominal beam position. If the beam is tilted with respect to the Silicon Detector, the rate of tracks with large fake impact parameters becomes excessive, giving rise to unwanted triggers. Monte-Carlo studies of ttbar and B events have shown that it is necessary to limit angular misalignment of the Silicon Detector with respect to the beam to less than ±200 μrad to limit the fraction of fakes to less than 5% for impact parameters of 100μ.

Lateral offsets should be kept below 1 mm to limit inefficiencies due to tracks crossing Silicon sectors. Lateral offsets of less than 1 mm are expected to be achievable by final realignment of the detector , and it is expected that orbit tuning can reduce residual lateral offsets to nominally zero after they are measured by the Silicon Detector.

The same angular constraints apply to the beam during stores, and the lateral position of the beam must be held steady to 30μ or so to avoid creation of an increased trigger rate due to apparent impact parameter increase. During Run I, CDF showed that lateral variations during stores did not typically exceed 40μ and angular variations were typically too small to measure. Angular variations store-to-store varied less than 100μrad. Preliminary DØ results for Run IIa are consistent with these values.

The present Run IIa Silicon Detector has already been shown to be aligned to the CFT to ± 70 μ at any individual silicon sensor. Since the overall length of the sensor staves of the Run IIb Silicon Detector is on the order of 1 m, such potential misalignment leads to well below 100 μrad of angular misalignment of the stave. It is intended to "recycle" the present mounting system between the CFT and the Run IIa Silicon Detector in such a manner that the quality of this relative alignment is not lost.

For this reason, and in view of the constraints on the required alignment, no type of dynamic alignment mechanism is contemplated for the Run IIb Silicon Detector. Precision fiducials will be provided on the silicon detector to enable the installed position of the device to be related to that of the existing CFT, so that the precision of this relationship can be verified after installation is completed

[25] U. Heintz, DØ Note 3516

4.7 Mechanical Infrastructure at DAB

4.7.1 Cooling system

DØ installed the two-piece Silicon Detector for Run IIa into the DØ fiber tracker in late 2000 and early 2001. Those two pieces are referred to the South half and the North half. Each half is read out by onboard electronics that generates heat which must be removed. Removal of that heat is performed by redundant chillers that circulate a glycol and water mixture in parallel closed loop systems with a common coolant reservoir. The coolant of the existing system is chilled to –10° C. For Run IIb, an additional system will be added to chill a portion of the coolant to -20° C.

Silicon in Layers 0-1 will be cooled to -10^{o} C while Layers 2-5 will be cooled to a minimum temperature of -5^{o} C. A temperature gradient may be allowed in Layers 2-5, with -5^{o} C at Layer 2 and a maximum temperature of $+5^{o}$ C at Layer 5. These temperatures will be achieved using a water-glycol cooling loop.

Use of the existing cooling system in place for Run IIa is possible, but with modifications to provide the two-tiered cooling needs of Run IIb. Currently the cooling system circulates 30% by volume ethylene glycol at -10^{o} C to the detector. For Run IIb, one glycol stream will need to be chilled to -20^{o} C for Layers 0 and 1 while a second stream will need to be -15^{o} C for outer Layers 2-5. Much of the existing piping and process control system can be preserved if a second chiller and supply line is provided for the colder silicon layers while allowing both streams to use the existing return lines in common. The existing chiller has a cooling specification of 4400 W at -10^{o} C and was tested to deliver 5500 W during actual tests at Fermilab.

To prevent freeze-out of coolant in the chillers, the freezing point of the circulating mixture must be 5.9^{o} C lower (10 F) than the fluid's control point temperature. Since coolant will be chilled to -20^{o} C, the fluid's freezing point must be -25.6^{o} C or lower. A glycol concentration of 41% by volume is chosen for the system, which has a freezing point of -25.9^{o} C. A 41% ethylene glycol, 59% water mixture by volume has the following properties which are used to define the Run IIb detector's flow rate and pressure drop limits if the existing system is to be used: at -20^{o} C, density = 1073.5 kg/m^3, viscosity = .01638 N/(m^2-s), vapor pressure = 0.7 mmHg.

To avoid risk of pump cavitation, the minimum allowable pump suction pressure is –10.4 PSIG. The calculation assumes a required pump NPSH = 8 FT and that the fluid vapor pressure is high (pv = 18.1 mmHg) at startup because the fluid is warm. The pump suction pressure is determined by system flow losses (the pressure drops both in the piping and the detector) and the elevation of the detector relative to the pump. The detector is about 3.96 meters above the pump intake. Piping flow losses are calculated using an Excel spreadsheet developed by Herman Cease for Run IIa but using fluid properties of 41% glycol, 59% water mixture at -20^{o} C. Table 17 (below) summarizes calculations by providing maximum pressure drops allowed across the detector for two possible flow rates, 10 GPM and 12 GPM.

Table 17 - Maximum Allowable Pressure Drop Across Detector

Coolant flow rate	**10 GPM**	**12 GPM**
P_s, minimum pump suction pressure to avoid cavitation	-10.4 PSI	-10.4 PSI
-(Head), due to detector elevation = 3.96 m	-6.1 PSI	-6.1 PSI
$-dP_{pipes}$, piping flow losses	6.1 PSI	8.3 PSI
Max allowable flow losses across detector, $\mathbf{dP_{det} = P_s - Head - dP_{pipes}}$	**-10.4 PSI**	**-8.2 PSI**

The table shows the tradeoff to be considered to cool the detector. If higher flow rates are desired, the flow passages must be far less restrictive to limit pressure drops. The calculations above are concerned only with piping downstream of the system's expansion tank, since only those components control the suction pressure at the pump. Flow losses in the piping are calculated for existing piping only. As discussed above, a new separate supply line is required to deliver –20^o C fluid to the inner layers, while the existing piping would supply fluid to Layers 2-5. The calculations therefore assume that the new parallel stream supplying coolant to the inner layers will have losses equivalent the existing piping supplying Layers 2-5.

4.7.2 Dry gas system

Temperatures inside the detector will be as much as 30^o C cooler than the maximum ambient dew point temperature (typically 10^o C) maintained by D-Zero's HVAC system. It is critical that moist ambient air be displaced from the detector volume with a dry purge source to prevent the formation of condensate and ice.

The existing dry gas purge and process control systems will be used for Run IIb, but the compressors, dryers, and cooling system will require appropriate maintenance after five years of continued service. The dry gas source proved failsafe for Run IIa through a 'What-If' failure analysis. An additional 'What-If' analysis is required if any changes are made for Run IIb. The dry gas system remains operational during all probable failure modes or has enough of a dry gas reservoir to continue to purge the detector until it is warmed above building dew point temperature. The purge source is reliable through extreme summer (40^o C, 100% relative humidity) and winter (-35 C) weather. The system is capable of delivering 60 SCFM of dry air purge. The maximum dew point temperature of the delivered gas is –60^o C.

4.7.3 Monitoring, interlocks, and controls

Monitoring, control, and interlock functions for the dry purge system and the silicon cooling system were added to the existing system commonly known as the DØ Cryo Control System for monitoring, interlocks, and alarming.

Mechanical piping and vessels of the dry gas and cooling systems were designed and fabricated with proper safety and relief devices so that the monitoring and interlock systems are not relied upon for personnel safety. All electrical loads have proper overload protection.

The Silicon Detector power system has an extensive *internal* interlock protection scheme provided by its power supply and processor control and data acquisition electronics

Thirty RTD temperature sensors were installed throughout the VLPC fiber barrel structure in order to track the fiber barrel temperatures as the Silicon system is cooled and its purge air flows are adjusted. Those thirty temperature sensors are displayed on the silicon computer graphics pictures.

4.7.4 Systems electrical power

DØ has backup electrical power provided by a diesel generator that starts automatically upon commercial power loss. The Silicon purge air compressors, the Silicon chiller cabinets, and the U.P.S. that supplies power to the Silicon cooling system control system are all on backup power. The silicon cooling system monitoring and interlock systems are powered by a U.P.S., which prevents power interruption to those control systems.

4.7.5 Existing chiller overview

There are two chiller cabinets, they have been designated chiller #1 and chiller #2. They are commercial units which contain a coolant pump, a chiller compressor, and the associated motor controls to run and control the unit. The temperature control is a stand alone single loop controller with a relay output and it is mounted on the chiller cabinet.

The chiller cabinet motor controls have been modified for remote interlock control. The remote interlocks have been implemented using solid state relays[26].

Each chiller has two bypass key-switches built into the cabinet. One key switch overrides the external pump interlocks while the other key switch overrides the external cooling interlocks. These were installed for emergency and diagnostic reasons. The keys to these key-switches will be administratively controlled.

4.7.6 Additional chiller overview

Two chiller cabinets will be added for the additional cooling loop expected to operate at -20° C. They have been designated chiller #3 and chiller #4. Either can be the active chiller with the

[26] Fermilab drawing 3823.112-EE-330338

other as a backup but not running. These will have interlocks and key switches similar to the original chillers.

4.7.7 Current process control system overview

The current process control system is based on a number of commercial Siemens Programmable Logic Controllers (PLC's) and is commonly referred to as the CRYO control system. These PLC's are capable of handling thousands of physical I/O through remote I/O bases. These remote I/O bases can have many types of modules installed in any of the slots for handling different types of field I/O. These PLC's are commercial computers which have many prewritten communication drivers available. Programming the PLC's is also done through commercial software.

The operator interface is based on the commercial distributed control platform of Intellutions FIX32. FIX32 provides computer alarms, graphical pictures with real time values, operator security, and historical collection of data. The use of FIX32 originated at DØ and is now commonly used throughout the Lab.

The Cryo Control System monitors and controls the Helium Refrigerator, LAR Calorimeters Cryo, Super conducting Solenoid cryo, Instrument Air, Vacuum, Building HVAC, WAMUS and Solenoid magnet power supplies, and the VLPC cryo.

4.7.8 Silicon cooling system integration into the current process control system

The Cryo control system was expanded with the addition of I/O base eleven on the South sidewalk and I/O bases seven, eight, and ten on the detector platform in order to pickup the physical field devices for the Silicon cooling system and dry purge air system.

The Silicon cooling system and dry purge air system logic programming were added to the PLC which has plenty of program capacity.

The Silicon cooling system and dry purge air system computer graphical pictures and database blocks were developed and added to the FIX32 system.

4.7.9 Silicon cooling system computer security

The Silicon Cooling System's computer security, along with all of DØ's other process control system's computer security are provided by a combination of Intellution's FIX32 and Microsoft's NT Operating System Platform.

The computer system's infrastructure is controlled and protected by Microsoft's Windows NT Domain Controllers. This infrastructure includes domain user accounts, server file protection, Remote Access Services (RAS), and distributed networking. This is the "DMACS" domain at Fermilab. There are currently three domain controllers, two at DØ and one at CDF. This domain is shared by many groups at Fermilab. The domain administrators control the domains user accounts and file privileges.

The process control system's security is provided by Intellutions's Fix32 and Fix Dynamics. This security is setup by the system developers who draw the pictures and build the databases. The system developers lay out their system based on a predefined set of rules. They then grant privileges to the users and operators who would need some control over these systems. These "privileges" are what allows some and denies others access to opening and closing a valve for instance.

Remote Process Control System access is provided by an NT RAS connection and Microsoft's NetMeeting. Remote access allows someone to view process data from home or elsewhere. The NT RAS security is provided by the NT domain controller, this security is essentially someone logging into the domain through a modem connection. NetMeeting allows someone to remotely take control of a workstations desktop. NetMeeting only allows an administrator to do this. The Process Control System security through NetMeeting is handled by NetMeeting, FIX32 or Dynamics, and the NT domain controllers. Other future remote access paths include the Internet i.e. a Website, however this is not well developed at this time.

4.7.10 Monitoring via the DAQ system

The DØ physics data acquisition and file system commonly referred to as the DZERO DAQ system will have access to the Silicon data along with all the other process control data. All the process data will be stored on a SCADA node dedicated to accessing and conditioning data just for the DAQ system. The DAQ programmers will be responsible for organizing a data polling list, then manipulating and storing the data in the physics file system. They may also choose to setup some sort of alarm system.

4.7.11 Interlocks

All interlock design and wiring practices use "failsafe" methods. That is a device must have positive feedback to its electronic circuits or it is considered "tripped". For example, a normally closed contact would be used on temperature switch in the field. This allows for a lost signal or a disconnected field device to generate a tripped condition. Discriminator modules are used in this system in order to convert an analog value into a discrete signal. These modules are all configured in their failsafe mode, which allows for loss of signal or transmitter failure to result in a tripped condition.

There is one exception to the failsafe practice in the Silicon Cooling System design. That is the control of the cooling circuit in the chiller cabinets. The chiller cooling control is called the Hot Bypass valve, when this valve is energized the chiller is not cooling. If the control signal is lost, the chiller would be forced into the cooling mode, since a solid state relay is used to control this circuit. This scenario has been countered by using this same DC control voltage that controls the Hot Bypass control, to control the main chiller power solid state relay. Therefore, if the DC control voltage were lost for any reason the entire chiller would shutdown.

Interlock Layers

The Silicon detector has two functional interlock layers. The primary power interlock system is embedded in the detector power supply and its control system. This system is capable of

monitoring temperature and other parameters and shutting down individual channels and groups of channels.

The secondary interlock system is based around the cooling system parameters and referred to as the external interlock system. The external interlock system is designed to protect the Silicon detector from temperature and dew point limits.

4.7.12 Alarms

The Silicon cooling system may run attended or unattended by operators. The alarms have been picked, programmed, and configured to be consistent with the other systems that the control system runs and monitors.

Alarm Layers

DØ incorporates a layered alarm strategy. There are typically three layers of alarms. The first is a computer alarm that notes when a parameter is slightly out of normal tolerance. The second is a computer alarm when a parameter is more than slightly out of tolerance. The third is an Auto-Dialer alarm when the parameter is at a point where immediate attention is necessary.

Computer Alarms

Computer alarms are generated by the FIX32 software mentioned earlier in this paper. An operator with the correct security privileges may set the alarm thresholds and also acknowledge these alarms.

A computer alarm can be routed and filtered by any of many FIX32 nodes throughout DØ and Fermilab. When a computer alarm occurs, all the FIX32 nodes that are set up to filter in the alarm area of a particular alarm will start beeping. This beeping will continue until the alarm condition is cleared and the alarm is acknowledged.

Auto Dialer Alarms

An operator with the correct security privileges may set the alarm thresholds and also acknowledge these alarms.

The Auto-Dialer alarm is generated by the PLC and a computer dedicated to running a software package called WIN911. This software package is capable of paging people's pagers with a numeric code as well as calling inside and outside the lab using the telephone system with a voice synthesized message. The Auto-Dialer is preprogrammed with a list of "experts" who can deal with the particular systems' problem that created the alarm. The Auto-Dialer will continue paging and calling people serially on this list until someone acknowledges the alarm or the alarm condition ceases.

The Auto-Dialer is what really makes unattended operation practical at DØ.

DAQ Alarms

All the PLC data from all process systems will be available to the programmers that program the DØ DAQ system. Once this data is picked sorted the programmers will likely set up a set of alarms. This assumption is based on last run's experience. The infrastructure for this data transfer is well defined and in progress of being implemented. The data sets remain to be defined.

5 READOUT ELECTRONICS

5.1 Overview

The readout system for the Run IIb silicon detector will be based on the new SVX4 chip and the existing Run IIa silicon data acquisition system. Sensors are connected to the outside world through hybrids with the SVX4 chips, and an external path consisting in turn of low mass jumper cables, junction cards, twisted-pair cables, adapter cards, and high mass cables followed by Interface Boards, Sequencers and VME Readout Buffers. A brief overview of the main ingredients of the readout system is presented in this section. Conservative solutions allowing for the fastest implementation of necessary changes were favored among different design options.

The SVX4 chip, designed as a joint DØ & CDF project, will be able to function in SVX2 mode and, therefore, will be compatible with the Run IIa readout electronics as discussed in detail in the next section. The chips will be mounted on hybrids. In the outer layers, the hybrids will be glued directly onto the silicon sensors. This allows for wire bonding directly from the chips to the sensors. The readout concept for staves in Layers 1 through 5 is shown in Figure 92. A "double-ended" hybrid design is chosen where chips are mounted on both ends of the hybrid and bonded to two different sensors. The hybrids are fabricated using thick-film technology on a beryllia ceramic substrate. All SVX4 chips on the hybrid are daisy chained for readout through one low mass digital Jumper Cable to the Junction Card. In Layers 2, 3, 4 and 5, the hybrid has 10 SVX4 chips and there are four readout cables per stave: two for axial sensors and two for stereo sensors. In Layer 1, 6-chip hybrids are used and there are three readout cables per phi segment.

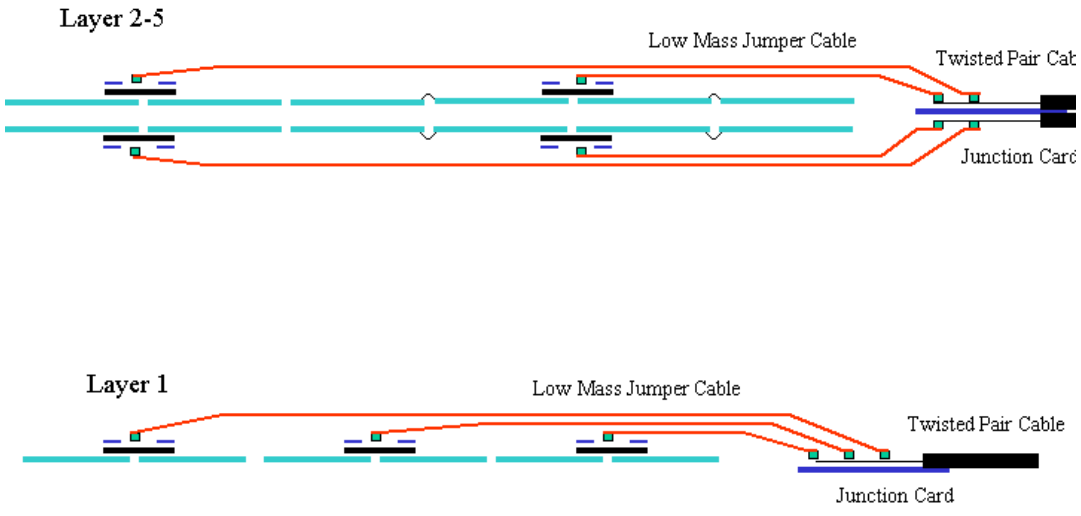


Figure 92 - Concept of readout for Layers 1 through 5

The innermost layer requires a substantially different design due to its very small radius and stringent requirements on the amount of material. For this layer, low mass analog readout cables

will couple the silicon and hybrids as shown in Figure 93. This allows the hybrids and silicon to be mounted independently, moving the mass and heat load of the hybrids out of the active detector volume. One 2-chip hybrid reads out one silicon sensor. To equalize the length of the analog cable between different sensors, the sensor closest to z=0 is connected to the closest hybrid. Digital jumper cables connect the hybrids to Junction Cards. While the added capacitance from the flex cable degrades the signal-to-noise (S/N) ratio, we expect to achieve a S/N>10 for the SVX4 with analog cable readout even at the end of Run IIb as was explained in Section 3.2. Section 5.3 discusses issues related to the analog cables.

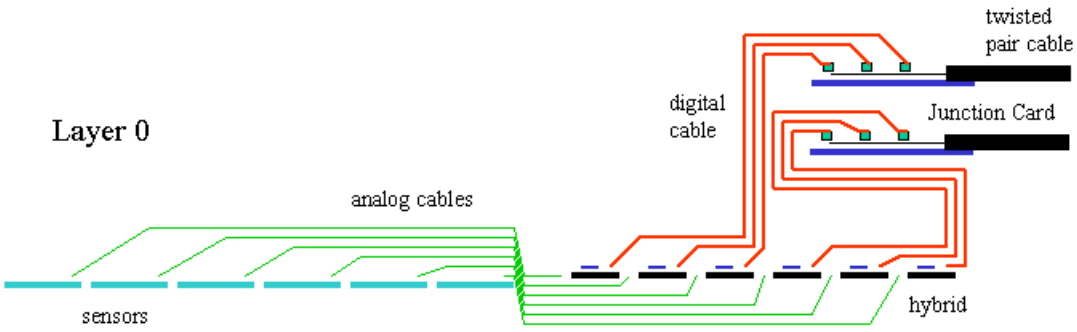


Figure 93 - Concept of readout for Layer 0

The total readout cable count is 888 with the cable count per layer given in Table 18. A detailed discussion of the hybrid and stave electrical properties is presented in Section 5.4.

Table 18 - Cable count per Layer

Layer	***Chips per hybrid***	***# readout cables***
0	2	144
1	6	72
2	10	96
3	10	144
4	10	192
5	10	240

A major consideration in the design has been to preserve as much of the existing Run IIa silicon data acquisition system as possible and to reuse the associated cable plant. Nevertheless, a few modifications are necessary to address two important issues:

1. The SVX4, produced in 0.25 micron technology will require lower operational voltage, 2.5 V as compared to 5 V necessary for SVX2. The allowed operational range of 2.25 – 2.75 V for SVX4 poses significant restrictions on the voltage drop in the power lines.

2. Modification of control signals are needed to accommodate the difference between the SVX2 chip and the SVX4 chip operating in SVX2 mode.

Figure 94 shows a block diagram of the Run IIa silicon data acquisition. SVX2 chips are read out with approximately 2.5 meter long low mass cables to the passive Adapter Cards located on the face of the calorimeter (Horseshoe). Interface Boards are connected to the Adaptor Cards with 6 meter long 80 conductor cables and serve as distributors of low voltages, bias voltages, data and control sequences for the detector. Interface Boards also monitor the temperatures and low voltages. Sequencers on the Platform provide clock and control signals for the SVX2 chips. The sequencers are also used to read out data from the chips and send them to the VME Readout Buffers via optical fibers. Only parts highlighted in gray will be modified for the Run IIb readout system. Adapter Cards and Low Mass Cables will be replaced with new components. Some firmware modifications in the sequencers will also be required as discussed in Section 5.11.

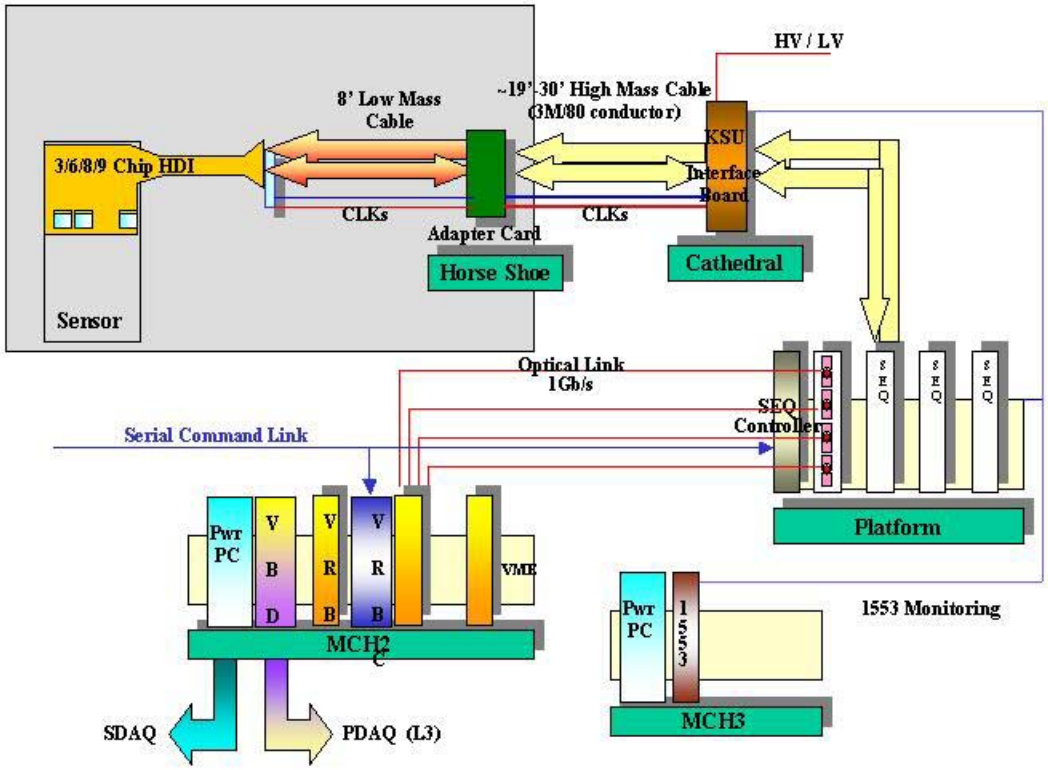


Figure 94 - Block diagram of the Run IIa silicon data acquisition system

Figure 95 shows the block diagram of the new components for the Run IIb data acquisition system. The Run IIa philosophy, having each hybrid connected to a single Interface Board channel, is preserved. However, the segmentation of this connection and the functionality of the intermediate pieces is different from that in Run IIa. A short low mass jumper cable starts from the hybrid and goes to the back of the detector where a passive junction card is located. The

junction card is connected to a new Adapter Card via a 2.4 meter long twisted pair cable. Data lines are driven differentially from SVX4 chips to the Adapter Card in contrast to the Run IIa approach which has single ended readout. Downstream of the Adapter Card, the lines are single ended.

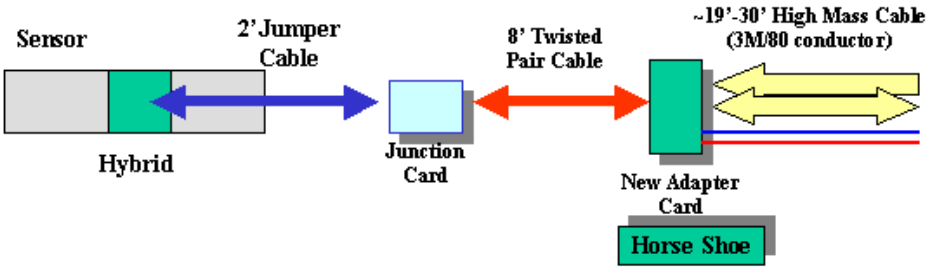


Figure 95 - Block diagram of the new components of the Run IIb data acquisition system

The Adapter Card is the key new component of the data acquisition accommodating most of the necessary modifications. It will perform the voltage regulation and will contain simple logic for the SVX4/SVX2 conversion as explained in Section 5.9. The Adapter Card is connected to the Interface Board with the existing 80-conductor cable. Some changes required for the Interface Boards are described in Section 5.10. Sections 5.6, 5.7, and 5.8 contain information about low mass Jumper Cables, Junction Cards and Twisted Pair Cables. Sections 5.12 and 5.13 have a discussion about low voltage and high voltage supplies and distribution. Results of simulations related to the readout performance are presented in Section 5.14. Grounding issues are discussed in Section 5.15.

5.2 SVX4 Readout Chip

The readout of the detector is accomplished by the use of the SVX4 readout chip, which is presently under development. The SVX4 is the last of a series of chips developed for silicon sensor readout by the FNAL-LBL collaboration. Earlier versions of such chips were the SVX-B and SVX-H (used in the readout of the first silicon vertex detectors of CDF), the SVX2 (used in the present DØ detector), and the SVX3 (used in the present CDF vertex detector). The SVX4 design thus draws heavily upon the experience gained from these earlier efforts and incorporates many of the desired features gleaned from this experience.

The SVX4 has 128 inputs with a 48 μm pitch, which receive the charge generated by 128 strips of a silicon detector. The input charge, for a well-defined period of time corresponding to a single beam crossing, is integrated and deposited in a capacitor of a switch-capacitor array called the pipeline. This pipeline has 46 cells, in which 42 can be used to store the charge, thus allowing the successive storage of the charge generated during 42 successive beam crossings. If an event is accepted by the Level 1 trigger framework during any one of the 42 beam crossings, the charge of the appropriate capacitor is digitized by an on board ADC, and the resulting digitized data is sent to the data acquisition system. The data can be read in a read-all mode (i.e. in its totality), in a sparsification mode (i.e. only channels above a certain threshold value), or in a sparsification mode with neighbors (i.e. in addition to the channels above threshold the

channels flanking them are also read out). The chip also has a deadtimeless feature, which allows for the concurrent acquisition of charge by the integrators and the pipeline while digitization or readout is taking place; this feature, which is the salient difference between SVX2 and SVX4, will not be used by DØ. Another difference between SVX2 and SVX3 is that only SVX3 has the dynamic pedestal subtraction capability, in which the gray code counter in the ADC is forced to start when the number of channels with the comparator firing reaches a preset value. By adjusting the preset value to an appropriate number, it effectively removes the average pedestal over the channels, resulting in the increase of dynamic range and the compensation of possible pedestal drift in time. The SVX4 inherits this capability.

The SVX4 will be produced in a deep submicron process (0.25 μm) by TSMC (Taiwan Semiconductor Manufacturing Corporation). Such submicron processing leads to a very small oxide layer which in turn results in a highly radiation tolerant device, without having to resort to any special manufacturing processing. Chips developed in such process (such as the APV25 chip for the CMS experiment and the VA1 chip for the Belle experiment) have been subjected to radiation doses exceeding 20Mrad with no sign of radiation damage, and will survive the expected doses for all layers of our detector. These submicron process chips require a power supply of +2.5 V, which is different from the +5V and +3.5V of the existing SVX2.

Because the SVX4 chip is a copy of the SVX3 chip used in the present CDF detector, it incorporates features that were not used in the SVX2 and are not part of the control and readout configuration of the Run IIa silicon data acquisition system. These features have to do mostly with the deadtimeless operation mode of the SVX3, which requires additional control lines and a dual clock (front end and back end clocks). However, it turned out that remapping our control lines to the ones required for the SVX3, which channels our clock to either the front end or the back end clock depending on the mode of operation of the chip, was adequate to operate the SVX3. A test board consisting of a single FPGA and simple transceivers was able to perform the required task, i.e. an SVX3 chip was read by the DØ sequencer board, as seen in Figure 96.

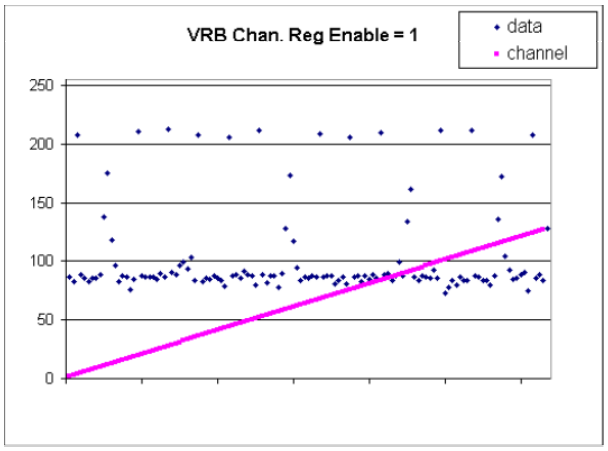


Figure 96. SVX3 chip performing in SVX2 mode with the DØ data acquisition system (November 2000)

As a result of this successful demonstration, DØ adopted the SVX4 chip designed by a FNAL-LBL-Padova team of engineers and has played an active and significant role in the design effort. The required remapping is shown in Table 19.

Table 19. Mapping between SVX2 and SVX4 readout/control lines

SVX 2				***SVX4***			
Mode				Mode			
INIT	ACQ	DIG	READ	INIT	ACQ	DIG	READ
BUS 0 PA RESET	BUS 0 PA RESET	BUS 0 PA RESET	Data 0	BUS4 PARST	BUS4 PARST	BUS4 PARST	Data4
BUS1 RREF-SEL	NC	HIGH	Data 1	BUS3 RREF-SEL	BUS3 RREF-SEL	BUS3 RREF-SEL	Data3
BUS2 PIPE-ACQ	BUS2 PIPE-ACQ	BUS2 PIPE-ACQ	Data2	BUS5 L1A	BUS5 L1A	BUS5 L1A	Data5
BUS 3 PIPE SREF	BUS 3 PIPE SREF	BUS 3 PIPE SREF	Data 3	BUS 6 PRD1	BUS 6 PRD1	BUS 6 PRD1	Data 6
BUS4 CNTR RESET	BUS4 CNTR RESET	BUS4 CNTR RESET	Data4	BUS2 PRD2	BUS2 PRD2	BUS2 PRD2	Data2
BUS5 RAMP RESET	BUS5 RAMP RESET	BUS5 RAMP RESET	Data5	BUS 1 RAMP RESET	BUS 1 RAMP RESET	BUS 1 RAMP RESET	Data1
BUS6 COMP RESET	BUS6 COMP RESET	BUS6 COMP RESET	Data6	BUS0 COMP RESET	BUS0 COMP RESET	BUS0 COMP RESET	Data0
BUS7 SR LOAD	BUS7 CAL INJECT	BUS7 N/C	Data7	BUS 7 CAL/SR	BUS 7 CAL/SR	BUS 7	Data7
MODE0	MODE0	MODE0	MODE0	FEMOD	FEMOD	FEMOD	FEMOD
MODE1	MODE1	MODE1	MODE1	BEMOD	BEMOD	BEMOD	BEMOD
CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE
TN	TN	TN	TN	TN	TN	TN	TN
BN	BN	BN	BN	BN	BN	BN	BN
CLK	CLK	CLK	CLK	FECLK	FECLK	BECLK	BECLK
CLKB	CLKB	CLKB	CLKB	FECLKBAR	FECLKBAR	BECLKBAR	BECLKBAR
DATA VALID	DATA VALID	DATA VALID	DATA VALID	OBDV	OBDV	OBDV	OBDV
PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN
PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT

This modification of control configuration can be accommodated by the existing DØ Sequencer readout module. In addition, the use of internal circuitry of the SVX4 allows the chip to operate in the so-called DØ mode. The circuitry can be turned on via an external wire bond to the digital voltage line. For operation in the CDF mode the wire bond must be connected to ground. In the DØ mode, using internal gating, the clock is sent to the appropriate section (front/back end) depending on the chip's internal mode. The same selector also forces the chip to use the PRD1, PRD2, L1A, and CALSR as inputs from the bi-directional differential data bus (for DØ) rather than their single ended dedicated input pads (for CDF). Thus, to use the existing DØ readout

sequencers the only major change required is a new adapter card with transceivers that will adapt the single-ended 5V signals used by the sequencer to differential 2.5V signals used by the SVX4.

In order to test and characterize the prototype chip in various aspects, we used three different test setups. The first setup at LBL is based on a pattern generator controlled by a Linux computer. In simplest terms this setup consists of two FIFOs, a clock oscillator, and an interface board to the computer. It is simple, flexible, well suited for quick extensive tests requiring frequent changes of download parameters and control sequences. However, the LBL setup does not allow clock frequency above 35MHz while the operational frequency is 53 MHz. The second setup is located at Fermilab, consisting of a sophisticated pattern generator with fine adjustment of timing (stimulus machine) controlled by a computer. Because of the capabilities of the stimulus machine, this setup has an advantage in detailed timing, frequency, and duty cycle studies. Most importantly this setup is capable of running at up to 100MHz clock frequency. The two setups above, therefore, are very much complementary. Detailed description of the stimulus setup and tests performed with the setup is available in Section 5.2.1. The third setup used for testing of SVX4 behavior on hybrids is based on the Standalone Sequencer and Purple Card. This setup is described in detail in Section 6.

During the SVX4 production the chips will also be tested on wafers before dicing. The corresponding setup is being prepared at Fermilab by the R.Yarema's group.

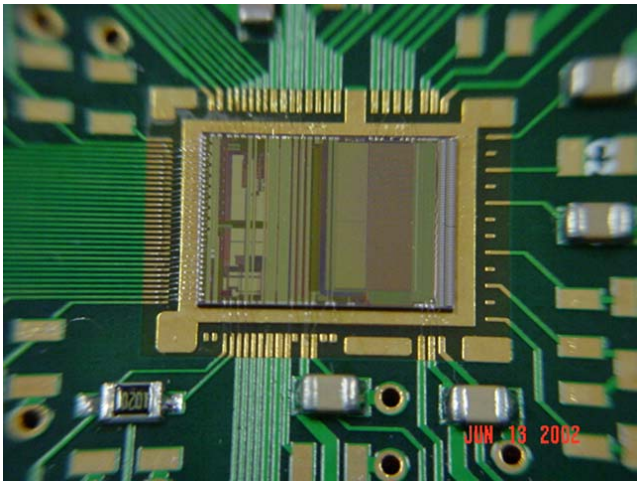


Figure 97. The photograph of the prototype SVX4 chip mounted on chip carrier board.

The first prototype chips were fabricated, and delivered to Fermilab and LBL in June 2002. Figure 97 shows the first prototype mounted on a chip carrier board in the LBL test setup. Since then, extensive tests have been performed using the three setups described above, as well as independent measurements of the front-end preamplifier. The most important conclusion is that the tests confirm the full functionality of the chips in both CDF and DØ modes. In the following, we list the highlights of some initial test results.

A preamplifier design with excellent frequency response, good reset time, good power supply noise rejection, and good noise performance has been identified. The overall noise of the analog section, i.e. preamp and pipeline combined, has been measured as $[300+41\times C(pF)]e^-$ with 100 ns

integration time and 70 ns preamp rise time, where the C is the input load capacitance. The preamp and pipeline gains have been found to be consistent with the specification. Non-linearity including both the analog and digital parts has been measured to be <0.3%. For the ramping voltage in the ADC, the offset level and the ramping rate are in good agreement with the expectation by the design. It is confirmed that the data output driver reproduces the input from the daisy chain, and passes the copied signal to the next chip. There are two configuration registers; a serial shift register and a Single Event Upset (SEU) tolerant shadow register. By changing the parameters stored in these registers, all bits have been checked to work as configured. The power consumption has been verified to agree with expectations. The different readout options, such as the sparsification mode, the dynamic pedestal subtraction, and ReadNeighbor feature have been tested.

An important issue to study was the frequency and duty cycle behavior. In the actual detector with a large number of channels, the duty cycle of the clock may be different from the ideal 50% form because of the long transmission lines of various lengths. This requires safety margins for the duty cycle and frequency of the clock. Studies are in progress to characterize the chip performance as function of frequency and duty cycle.

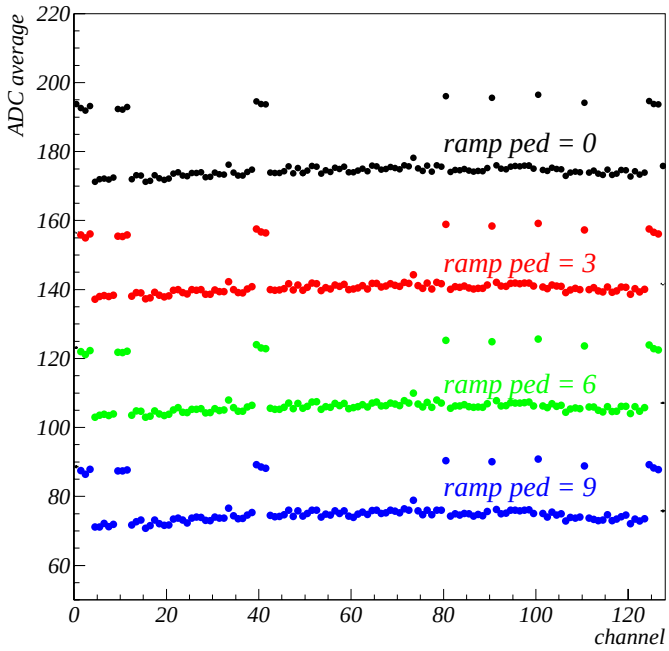


Figure 98. Average of ADC counts for 100 events across the channels. The calibration charge is injected to the channels with higher ADC counts. The offset of ramping voltage in the ADC has changed, and thus the digitized ADC counts for the calibration charge (= difference between the charged injected channels and the others) is constant.

Figure 98 and Figure 99 show the ADC counts for all 128 channels with some configuration parameter settings. The calibration charge is injected to the channels with higher ADC counts. It is verified that variation of the configuration parameters correctly affects the output ADC counts, as seen in the two figures.

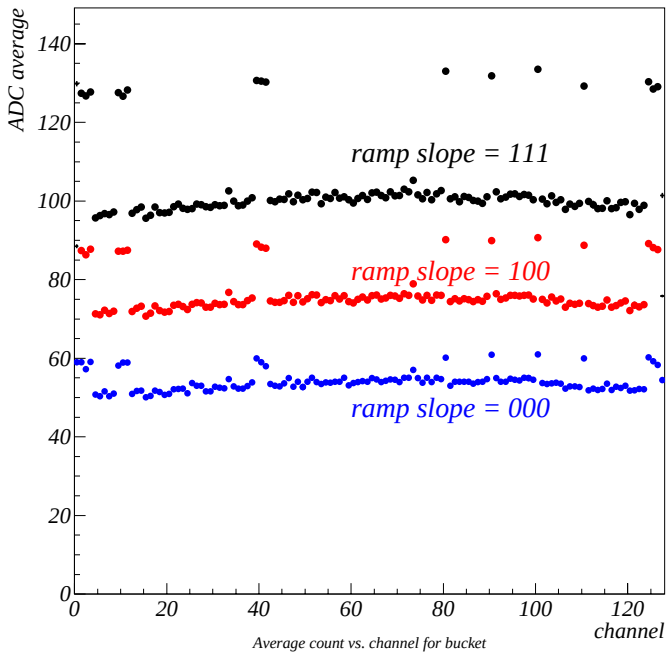


Figure 99. Average of ADC counts for 100 events across the channels. The calibration charge is injected to the channels with higher ADC counts. The ramping rate in the ADC is varied. This gives the change in both the digitized ADC counts and pedestals.

An irradiation test for the analog front end part had been conducted for the test chip, which consisted of only preamp and the pipeline, using a ^{60}Co gamma ray source. While the test result did not show any significant performance degradation, the prototype SVX4 chip should also be irradiated. We are planning two separate studies. The first one is irradiation by hadron beam for testing the shift register and the Single Event Upset (SEU) tolerant shadow register. To check if there are any corrupted bits in the shift register during exposure, the chip will be kept running and shift register values will be read out continuously. The shadow register also has to be examined at the same time. The second test will check sensitivity to total doses. This test will use a ^{60}Co gamma source. These two tests will be performed in September 2002.

As shown above, no fatal failures or bugs of chip operation have been found so far. However, some minor bugs were revealed. These include modification of ADC control sequence to facilitate switching between Acquire and Digitize in DØ mode, modifications of two bit assignments in the data field, and layout modifications in ADC for better pedestal uniformity across the channels. The fix list is being created, and the revision of the design is in progress now. The target date of pre-production submission for the next prototype is mid-November 2002.

5.2.1 SVX4 tests with Stimulus Setup

The stimulus test stand was originally designed for testing the SVX2 silicon readout ASIC and then upgraded for SVX3 prototyping and testing. We have modified this system for SVX4 testing.

The stimulus test stand consists of a PC with a GPIB interface card, a DAC-812 and a PCL-710 digital counter both connected through an ISA port. A custom DAQ program (SVXEval) was written for Windows 9x. The program algorithmically constructs patterns in memory and transmits them via GPIB to a Tektronix HFS 9003 Stimulus System. The PC also programs a HP 16500B Logic Analysis System over GPIB. The PC is a 200 MHz Pentium with 64 MB of RAM and is running Windows 98. We show the entire system in Figure 100.

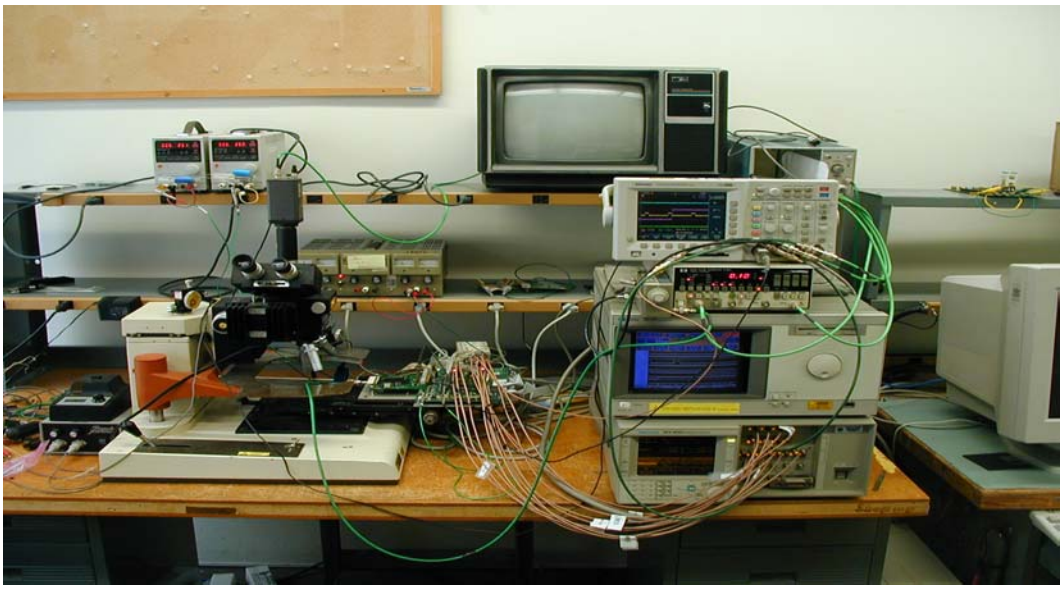


Figure 100. The Stimulus Test Stand. The PC is located to the far right. The Stimulus System is located next to the PC below the Logic Analysis System, HP Pulse Generator, and Tektronix TDS 3034 Oscilloscope (in order from bottom to top). Cables connect the Stimulus System outputs to the SVX4 Adaptor Board located in the middle which is connected to a SVX4 chip carrier. The Adaptor Board and Chip Carrier are mounted on a movable table of the Rucker & Kolls Probe Station that has a Bausch & Lomb MicroZoom microscope connected to the television. The power supplies for the Adaptor Board and SVX4 chip can be seen as well as the power supply to two Picoprobes that are used to probe pads located on top of the SVX4 chip itself.

The Stimulus System sends patterns to the SVX4 through a custom designed interface board and has a maximum speed of 630 MHz. The frequency for normal operation is 530 MHz which allows an ability to change the waveform at the level of 2 ns. The Stimulus System has a total pattern memory of 64 K vectors which allows a pattern length of 128 μs. In practice, the pattern memory is divided into different cycles of SVX4 operation and these individual patterns can be repeated indefinitely.

The HP 16500B Logic Analysis System contains a 4 GHz/1 GHz Logic Analyzer along with a 2GS 32K Oscilloscope. The Logic Analysis System has two HP pods with flying-lead probe tips that are used to monitor the signals being sent to the SVX4 chip via the SVX4 adaptor board and the data output from the SVX4 chip. Each pod has 8 data lines which gives us the ability to monitor 16 different signals in the system. One probe is used to monitor control signals and the other is used to view the data from the SVX4 chip. We are able to graphically view the waveform being downloaded to the chip and the data coming from the chip.

The SVX4 Adaptor Board, designed by the University of Kansas, has multiple functions. Because the Stimulus System cannot generate enough control signals, an EPLD located on the Adaptor Board is used to generate the extra control signals necessary for proper SVX4 chip operation. The Adaptor Board properly terminates the signal and bus lines of the SVX4 chip, contains test points which give convenient connection points for the flying-lead probe tips of the Logic Analysis System, and allows for dual mode (DØ/CDF) operation of the SXV4 chip. We show the SVX4 Adaptor Board in Figure 101.

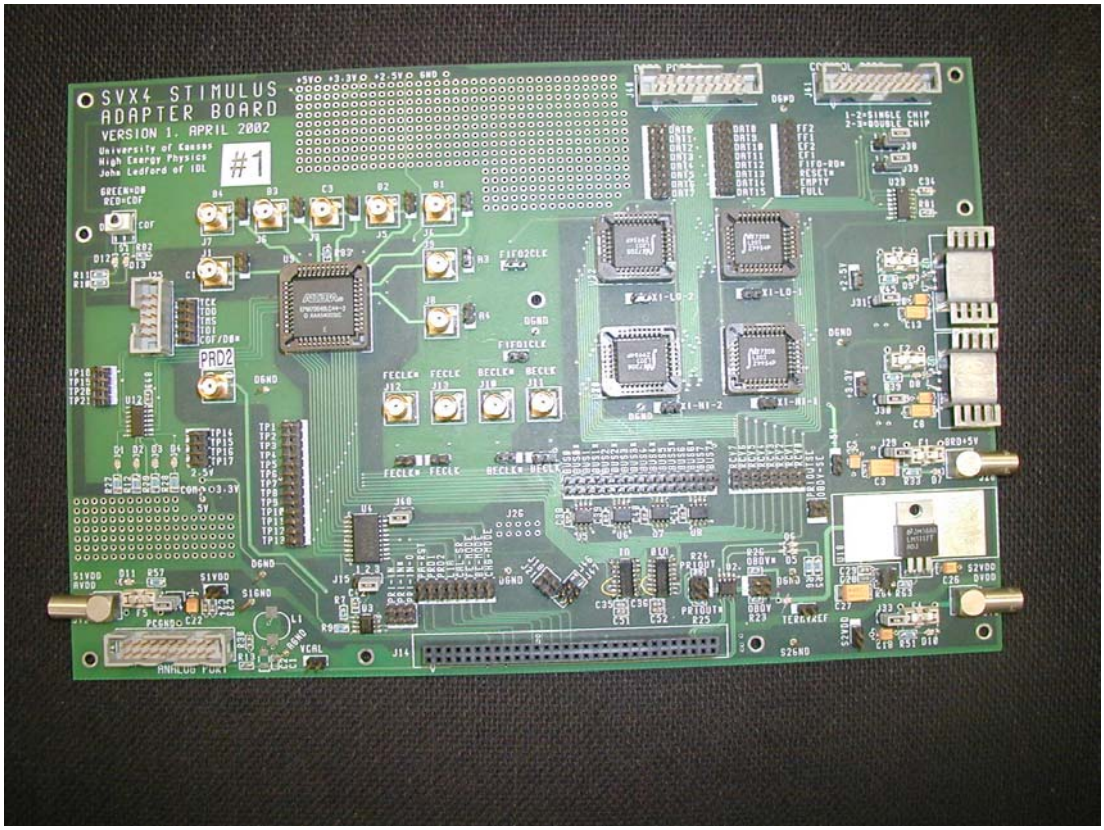


Figure 101: The SVX4 Adaptor Board. The Adaptor Board is used to interface the Stimulus System with the SVX4 chip. This board contains an Altera EPLD which contains a finite state machine used to generate the extra control signal for proper SVX4 operation. It also contains four FIFOs that are used to buffer data between the chip and the computer. The 60 pin connector in the middle of board is the connection used to the SVX4 chip carrier. The Lemo connectors at the sides of the board are used for power connections.

In Figure, we show a cartoon representation of the hardware for the Stimulus Test Stand. The computer sends a pattern to the Stimulus System via the SVX4 Adaptor Board. The SVX4 chip is mounted onto a carrier board. The data from the chip is stored in FIFOs on the Adaptor Board until the computer can read out the data. The Logic Analyzer has two pods which probe test points on the Adaptor Board and gives a graphical representation of the waveform and the data output of the SVX4 chip.

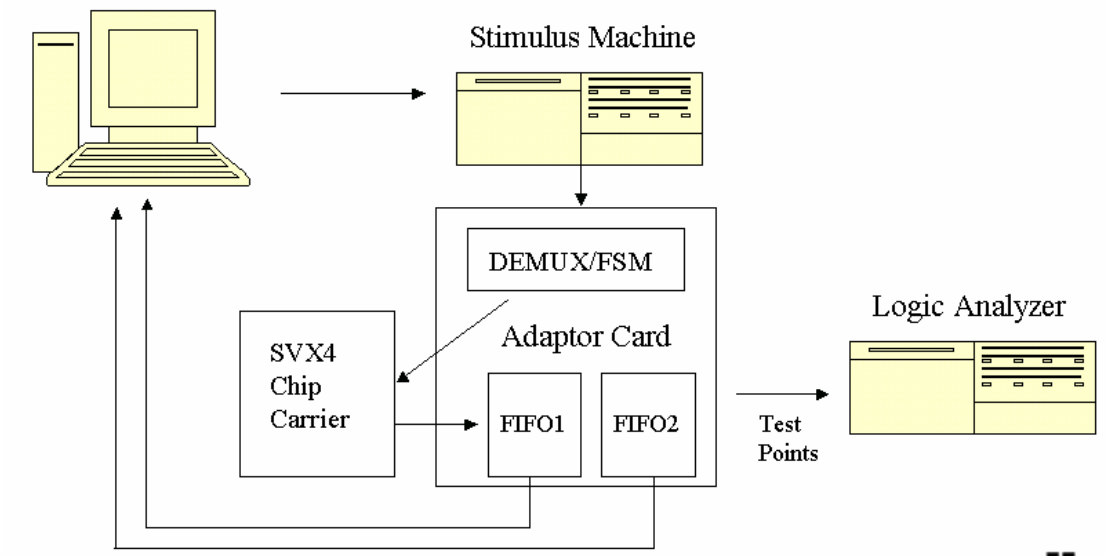


Figure 102. Cartoon representation of the Stimulus Test Stand. The PC is connected to the Stimulus System and the Logic Analyzer through GPIB. The SVX4 Adaptor Board is in the middle with the demultiplexer/finite state machine (programmed inside the EPLD on the board

The waveforms that are downloaded to the chip are generated algorithmically and can be altered by a graphical waveform display/editor provided by the software. We show the waveforms for the DØ mode and CDF mode of the SVX4 chip in Figure 103.

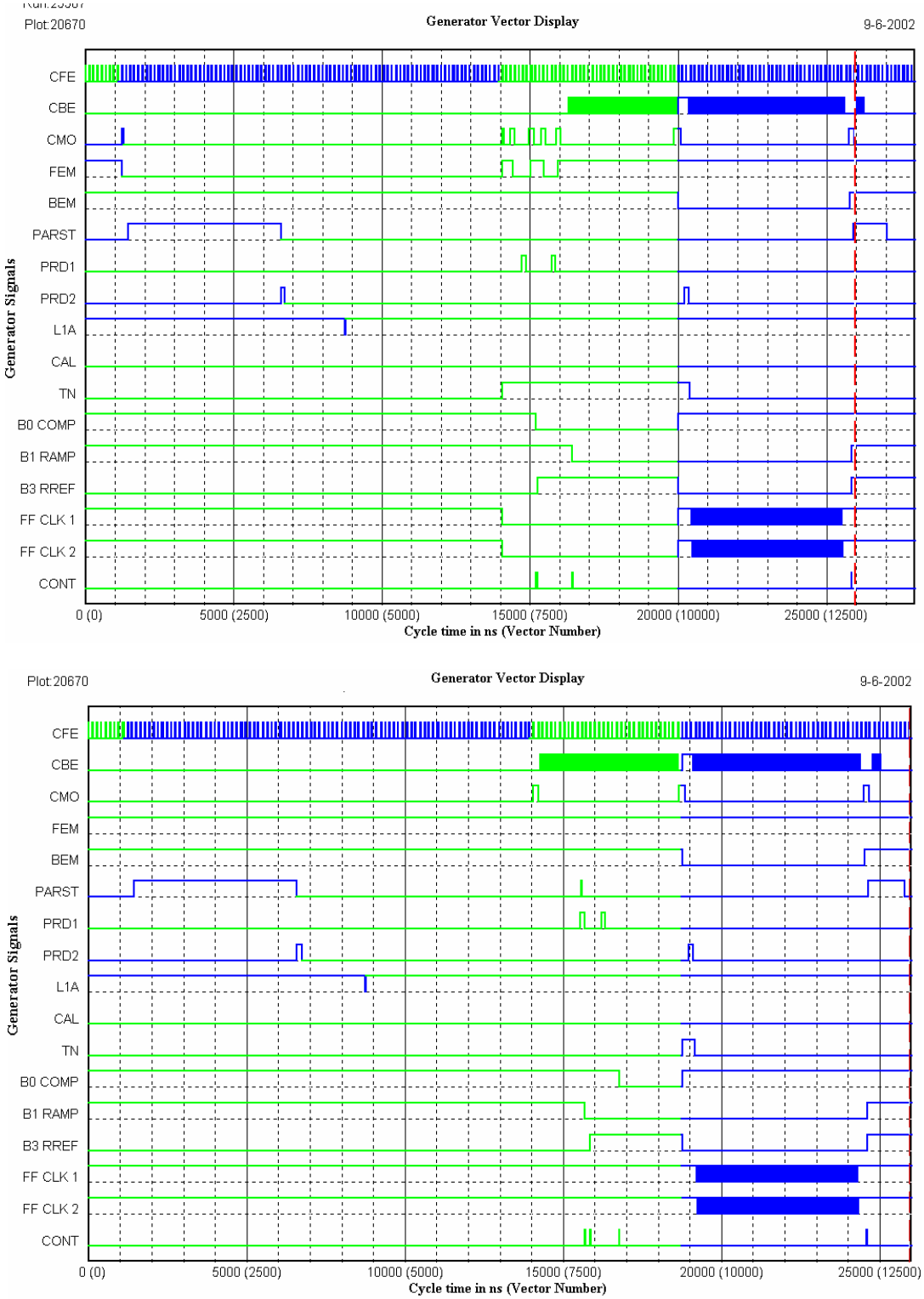


Figure 103. DØ (upper) and CDF (lower) waveforms. These waveforms are generated algorithmically by the DAQ software and are download to the SVX4 chip via the adaptor board. The three signals corresponding to setup of the ADC (COMP, RAMP, and RREF) are shown here only for understanding the timing. The actual signals are generated by the EPLD by using the control (CONT) signal. The FIFO clocks are no longer used.

The stimulus system is fully operational and we are proceeding with the SVX4 performance tests. An interesting measurement done with the setup is study of the current consumption of the SVX4 during an entire data cycle. A data cycle consists of entering the Acquire cycle followed by the Digitization cycle and Readout cycle. We used a calibrated current probe on the individual power supplies (AVDD and DVDD) and then we connected both power supplies together and measured the contribution from both the front-end and back-end from the single supply. This is important because it is necessary to know what the average and peak currents that the power supplies must be able to generate when powering a stave inside the detector.

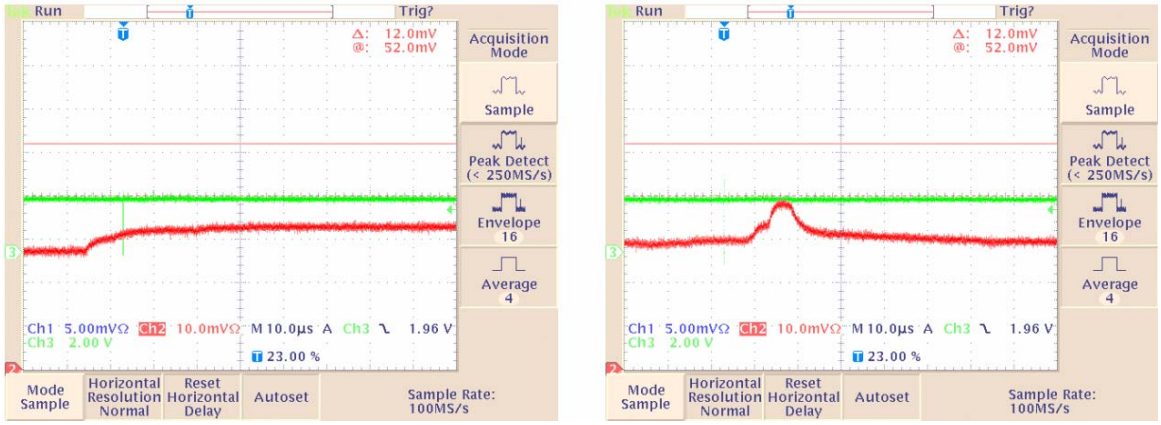


Figure 104. Current consumption of the SVX4 Version 2 chip. The left hand picture is the current consumption for and independent supply connected to AVDD=2.5 V. The vertical scale is 20 milliamps/division with zero is the lower left corner. The right hand picture is the current consumption of an independent power supply connected to DVDD=2.5 V. The scale is also 20 milliamps/division with zero in the lower left corner.

For consistency we powered AVDD and DVDD from one power supply to measure the combined current draw from the front-end and back-end during one data cycle. This is shown in Figure.

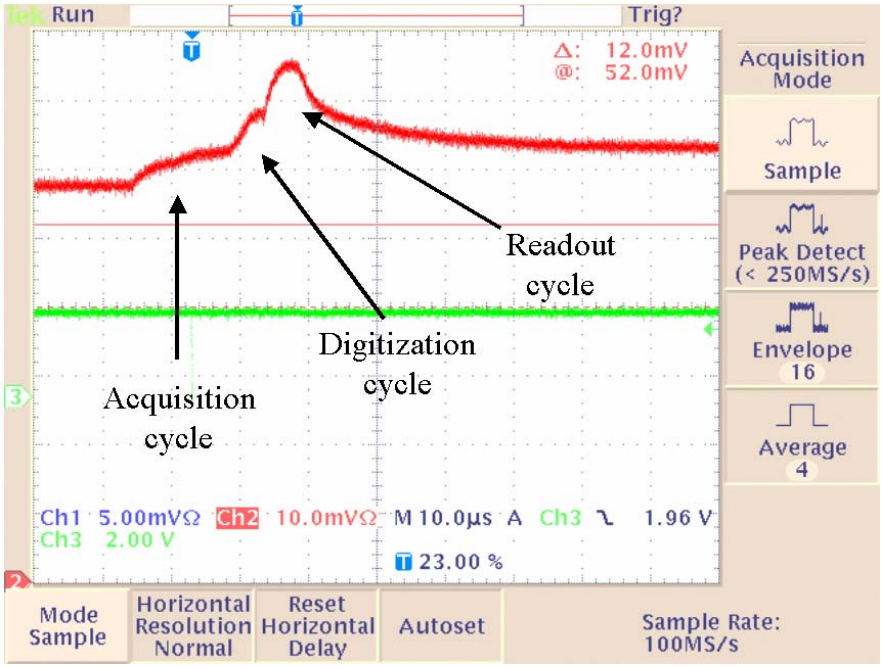


Figure 105. Current consumption of the SVX4 Version 2 chip. The vertical scale is 20 milliamps/division with zero is the lower left corner. Both AVDD and DVDD are connected to the same power supply: AVDD=DVDD=2.5 V. The scale is also 20 milliamps/division with zero in the lower left corner. The sum of the individual currents sum to the total within a few percent.

5.3 Analog Cables

In the current design of Layer 0, the analog signals from the silicon sensors are transmitted to the hybrid containing the SVX4 chips by flexible circuits up to 435 mm long with fine-pitch copper traces. While very attractive because of material and heat removal from the sensitive volume, this approach represents a considerable technical challenge. Addition of the analog cable deteriorates the noise performance of the silicon sensors. Procurement of the flex cables and the complicated ladder assembly are other non-trivial issues. Nevertheless, a similar design is used by CDF for the readout of the innermost layer L00 in the Run IIa SVX detector, which can be considered as a proof of technical feasibility.

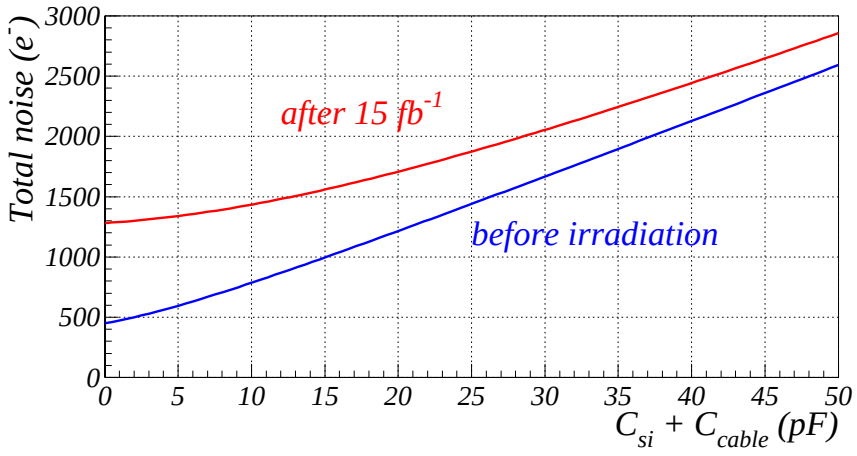


Figure 106. Expectation for the total noise as a function of sum of sensor and cable capacitance.

One of the most important aspects in the design and technical realization of a long analog cable is the capacitance between the traces, which has to be as small as possible. Any load capacitance will contribute to the noise seen by the preamplifier. Our design goal is to maintain a S/N ratio of better than 10 for Layer 0 after irradiation corresponding to 15 fb^{-1} of data. Figure 106 shows the expected noise level as a function of capacitance summed over silicon sensor and analog cable. Assuming that a minimum ionizing particle creates 22,000 electrons by traveling through a silicon sensor with the thickness of 300 μm, the total capacitance must be kept below 33 pF to maintain the S/N better than 10 given the measured SVX4 noise performance. The 8 cm long silicon sensor will have about 10 pF of capacitance. This means that the analog cable is required to have capacitance less than 23 pF or 0.53 pF/cm.

The flexible dielectric substrate of the cable affects the capacitance. The material of choice in high-energy applications is polyimide such as Kapton HN with a dielectric constant of 3.5 at a frequency of 1MHz. This material is radiation hard with good mechanical and electrical properties. Other synthesized polyimide materials on the market achieve a lower dielectric constant by adding halogens. They are not radiation hard and are not in compliance with CERN and Fermilab fire safety regulations. Although materials like polyethylene or polypropylenes are used in the flex industry and possess a lower dielectric constant, they are also not radiation hard up to the 10-15 MRad level, to which the innermost layer of the silicon tracker will be exposed. The material choices for the flex cable are, therefore, limited to the standard polyimide.

Considering the tight schedule and the technical difficulties, we investigated a design that allows a manufacturer to produce cables reliably, and also satisfies the capacitance requirement.

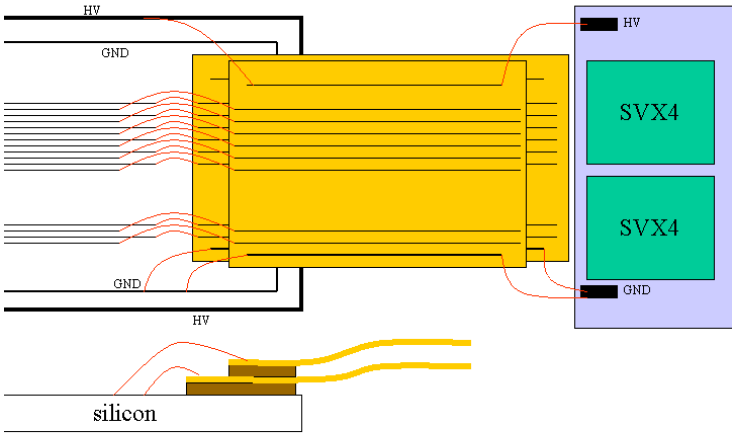


Figure 107. Schematic view of the proposed connections between the sensor, analog cable and the hybrid for Layer 0

Figure 107 shows the schematic view of the proposed arrangement for the sensor, analog cable and the hybrid. Two cables with constant 91 micron pitch are laminated together with a lateral shift of 45 μm. This works effectively as a cable with 45 μm pitch. We think this is a simpler alternative to the L00 approach which has fan-in and fan-out regions adapting the 45 micron pitch to 100 micron pitch. We also investigated the dependence of the cable capacitance on the trace width to understand the trade-off between the reliability and performance.

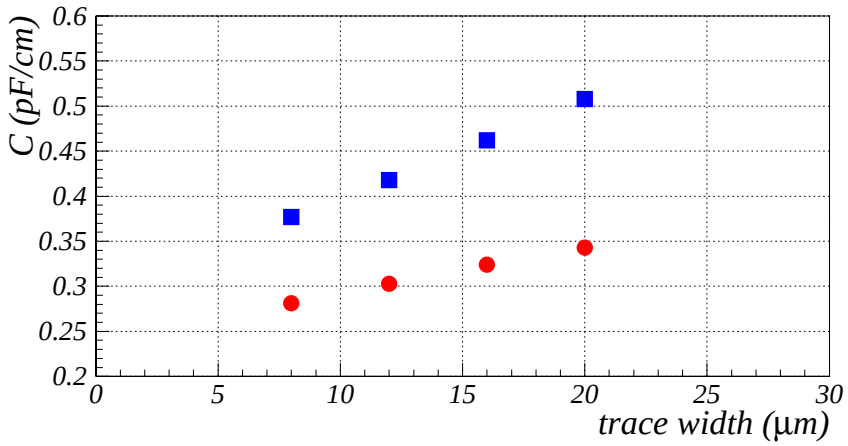


Figure 108. Capacitance calculations by ANSYS. The capacitance of one trace to all other traces is shown as a function of trace width. The blue squares represent 50 μm trace pitch, and red circles 100 μm

Figure 108 shows the expected capacitance for various trace width and different pitch by finite element calculations using the ANSYS program. The height of the traces is assumed to be 8 μm

in the calculations. It turns out that the 100 μm pitch cable reduces the capacitance by 30% compared to the 50 μm pitch. Besides, the dependence on the trace width is weaker for the 100 μm pitch, correspondingly 0.0052 pF/cm/μm for the 100 μm pitch and 0.0109 pF/cm/μm for the 50 μm pitch. Based on this result of the calculations, we adopt the following design as a baseline: 16 μm trace width and 91 μm constant pitch with no fan-in/out region. The 16 micron trace width is a factor of two larger than the trace width of the L00 CDF cable, which we expect to result in increased reliability and higher production yield of the cable. In the final design the pitch is reduced from 100 to 91 μm because the HV trace must hold up to ~1000 V and, therefore, needs to be separated by more space on the cable.

In order to reduce the capacitance contribution from the adjacent cables, a spacer will be placed between the cables. A candidate for the spacer material is polypropylene mesh sheet with dielectric constant 3.5. Taking into account the 50% volume occupancy due to the mesh structure, and the possible reduction of the amount of material by punching more holes, the dielectric constant can be effectively as low as 1.5. The thickness of the spacer would be 200 μm at maximum because of mechanical constraints. The capacitances calculated by ANSYS for the configuration with two cables and a spacer are summarized in Table 20.

Table 20. Capacitance in one trace relative to all other traces calculated by ANSYS. The first line is for a single cable, and the other for the configuration where two cables are laminated together with the 200 μm thick spacer. The first column is the dielectric constant for the spacer.

ε_r of spacer	Capacitance (pF/cm)
Single cable	0.339
1	0.342
2	0.466
3	0.585

This result indicates that separating two cables by a proper spacer can maintain cable capacitance below the required value. From this encouraging result, DØ adopts the method of using two 91 μm pitch cables for one chip readout, in which a pair of cables with a spacer functions as a 45 μm pitch cable. Hence the trace pitch can be almost twice that of the old design, resulting in relief of the technical difficulty.

Based on good prior experience with high density interconnects (HDI) from Dyconex Inc. in Zurich, Switzerland, we contacted them in May 2001. After a few iterations of their prototyping and our technical evaluation, in July 2002 they delivered 27 good prototypes. Figure 109 is a photograph of one of the prototype cables. The copper traces are gold-plated, and the bonding pads have been confirmed to be bondable. Out of the 27 cables, 25 cables satisfy the specification in the number of open traces. While the specification is that 128 traces out of 129 (one trace is spare) are continuous, 16 cables have no opens, and 9 cables have 1 open. Another important requirement is capacitance. The specification is <0.40 pF/cm. The capacitance of one

trace to neighboring two traces has been measured to be 0.30 pF/cm. From ANSYS calculations, 10-15% of increase is expected from contributions besides the two neighbors. Measurements on the old prototype cable with all the traces were shorted together had verified this increase rate. Therefore, 0.35 pF/cm is a fair estimate of the capacitance. This is within the specification.

Figure 109. Photograph showing the edge of the most recent prototype cable.

5.3.1 Layer 0 Prototype

In Layer 0, the tight space constraints and heat dissipation require us to use a low-mass analog cable to couple the silicon sensor and the SVX4 chip mounted on the hybrid. As discussed in Section 5.3, special attention has to be paid to the capacitance increase caused by the long analog cable, to avoid degradation of the noise performance. In addition, the experience of the Run IIa L00 in CDF reveals other possible noise sources: noise due to capacitive coupling between the detector and nearby floating metal such as cooling tubes, and also RF pickup noise by the analog cable.

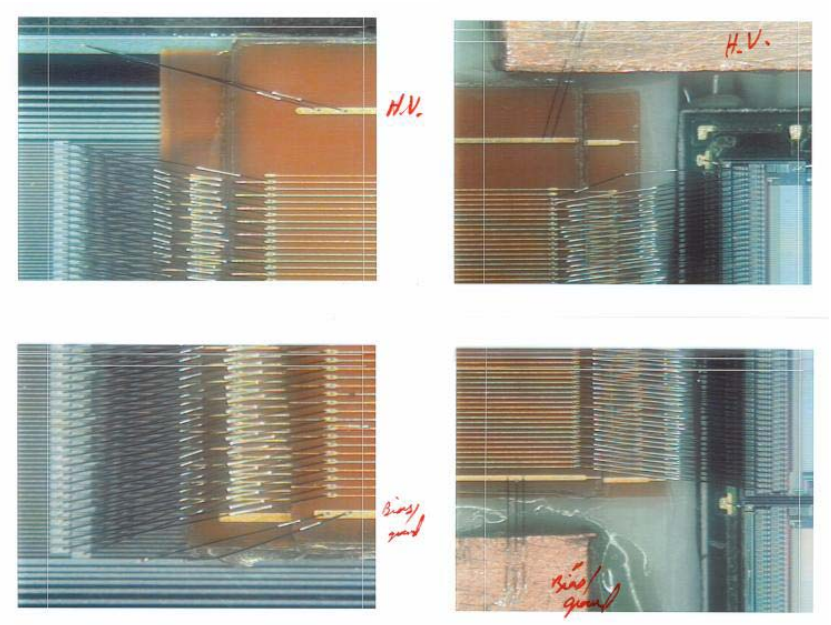


Figure 110. The photograph of the connected region between the sensor and the analog cable (left) and between the cable and the chip (right).

In order to study the effect of these additional noise sources, a L0 prototype was assembled from a L0 prototype sensor manufactured by ELMA, an analog cable manufactured by Dyconex, and a Run IIa hybrid for the readout. The wire-bonding regions for the sensor to the analog cable and for the cable to the chip are displayed in displayed in Figure 110. The L0 prototype fixture is put inside a plastic box for light tightness, and is well insulated to avoid any capacitive coupling to the assembly. There are three SVX2 readout chips mounted on the hybrid. Out of the three, two are used to read out the signal from the sensor through the analog cable, while the remaining chip does not have any input loads, and serves as a reference noise level in the test setup. In the noise study described in this section, the noise level is defined as the RMS of pedestal distributions for 100 events.

Apart from the electrical measurements described below, this prototype is a successful demonstration of the proposed arrangement for analog cables. The prototype allowed us to come up with specifications on exact dimensions for the final system and to verify the feasibility of bonding between the cables and the sensor and between the cables and the hybrid.

First we measure the noise level in an electrically quiet environment (accomplished by wrapping the whole fixture by aluminum foil connected to ground), to estimate the amount of additional noise due to the load capacitance of the analog cable. The left plot in Figure 111 shows the noise level for each channel. The projection in each chip is shown in the right. From Gaussian fits of the distributions, the average noise level is 2.2 ADC counts, compared to 1.4 ADC counts in the third (reference) chip. Assuming one ADC count is equivalent to 1000 electrons, the increase of noise level can be translated as 800 electrons. Using the fact that a minimum ionizing particle creates roughly 22,000 electrons in a sensor, the observed noise from the additional capacitive load is acceptable even for the old SVX2 chip.

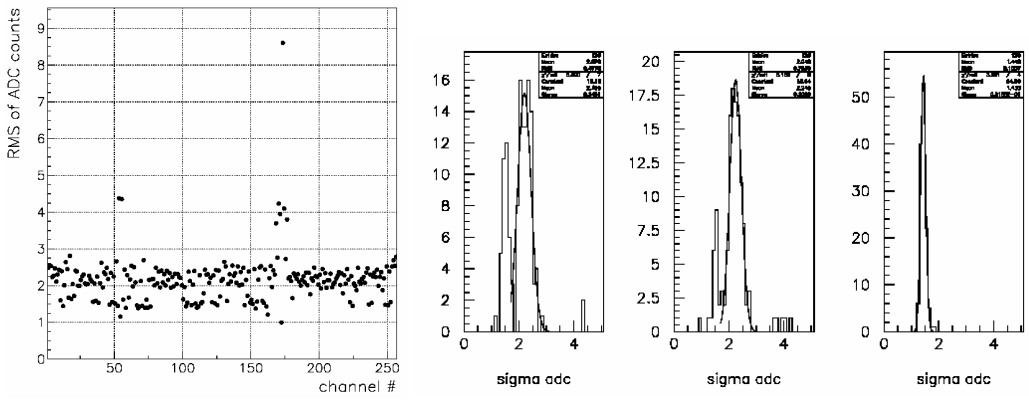


Figure 111. The noise level for each channel (left). The channels with very high (or low) noise are caused by wire-bonding failure. The right plots show the projection of the left one for each of the three chips mounted on the hybrid. The first and second chips are used for the readout, while the third is a reference for the noise level.

The second study is a comparison of the noise levels with and without external shielding. Figure 112 shows the noise for each channel without the shielding. The noise level is increased by 1 to 13 ADC counts (corresponding to 1000 and 13,000 electrons, respectively), depending on the location. This noise increase implies the existence of RF pickup. Another interesting observation is the wing-like shape of the noise distribution. This is attributed to a shielding effect by traces themselves in the middle of cables, where neighboring traces work as a shield for each other; this effect is less significant at the edges of cables. This result unfortunately indicates that the analog cable indeed works as an antenna, and that shielding of the cable is crucial.

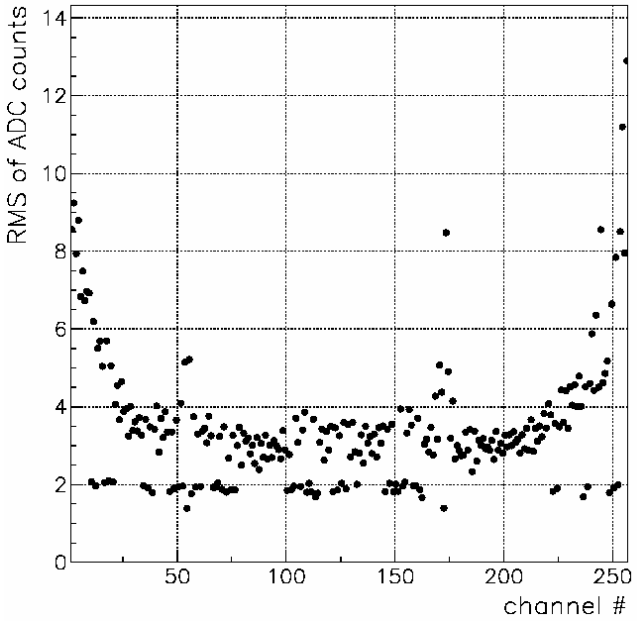


Figure 112. The noise level for each channel. The L0 prototype fixture is not shielded at all.

The next study is for the noise due to capacitive coupling of external sources to the analog cable. We placed a piece of aluminum foil under the analog cable. The aluminum foil was not grounded and thus was floating. Figure 113 shows the noise level for each channel, clearly indicating the capacitive coupling between the analog cable and the aluminum foil by two distinctive features. First, there is an even-odd effect. This comes from the difference in distance between the floating aluminum piece and the signal traces on the cable, i.e. one cable is laminated on top of the other and thus its distance is twice as great. Second, higher noise is observed near non-connected channels (those were bonding failures). The non-connected channels have signal traces without effective grounding through the preamplifier, leading to stronger capacitive coupling to the aluminum foil.

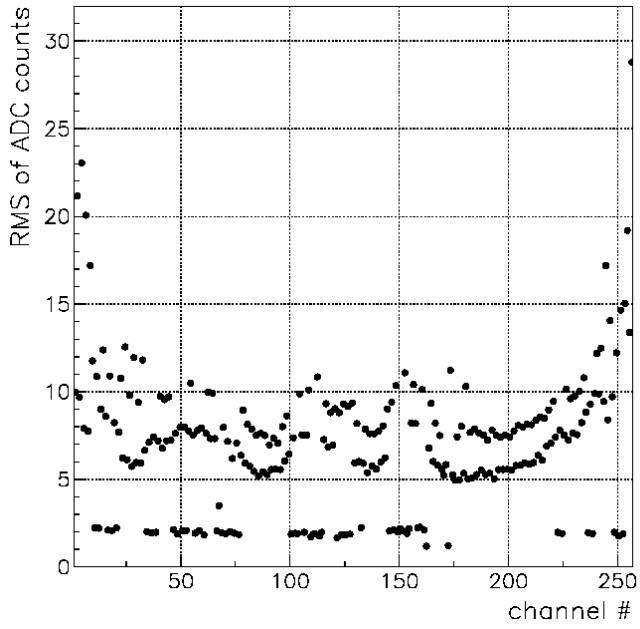


Figure 113. The noise level for each channel. An aluminum piece without grounding connection is placed under the cable.

Figure 114 shows the pedestals and noise for a different prototype with a grounded shield. As one can see the grounding removes the noise and pedestal structure and reduces the noise to a level expected from the capacitive load.

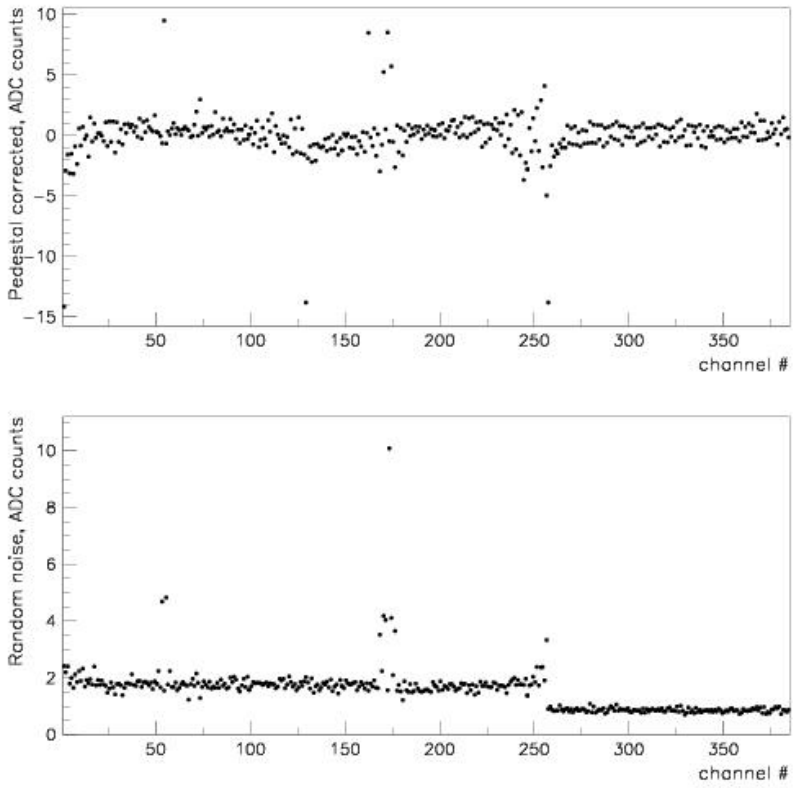


Figure 114. Pedestal and noise for L0 prototype with grounded shielding

From the test results above, a particular concern for L0 is the proximity of sensors to highly conductive K13C carbon fiber, which will be used for cooling tubes and mechanical support structures. These elements have the potential to produce strong capacitive coupling to the sensors, similar to what CDF experienced in Run IIa with L00 cooling tubes, and to what we have seen in the L0 prototype. Therefore, it is imperative that all carbon fiber in the detector be effectively shorted to the bias filter grounds to prevent capacitive noise transmission to the sensor readout.

A test was conducted to determine the feasibility of shorting a prototype L0 carbon fiber cylinder to a filter ground plane. The carbon fiber was driven with the source power from the network analyzer. A sensor/filter mockup constructed of aluminum and Kapton layers was mounted on the cylinder with the network analyzer input wired to the sensor aluminum layer, and both the source and input grounds wired to the filter plane. Transfer functions to the sensor were measured with different configurations for shorting the carbon fiber to the filter plane. Strips of 1 μm thick aluminized Mylar, 0.5 mil aluminum, or copper tape were attached across the filter and carbon fiber. The effectiveness of the grounding strips was tested with and without additional copper tape coupling to the carbon fiber. The aluminized Mylar strips were minimally effective in reducing power to the sensor. Aluminum and copper strips performed equally well. The power reduction was independent of the number of strips, but proportional to the amount of copper tape used to couple the strips to the carbon fiber, up to a maximum reduction of 40 dB at

1 MHz. Further studies determined that aluminum foil embedded in the carbon fiber provides very good coupling for grounding to the filter plane. The embedded aluminum will have 2mm wide strip extensions that will be folded over and shorted to ground pads on the filter. Further details of the carbon fiber grounding studies can be found in 5.15.

Based on the grounding scheme studied above, we plan to assemble another L0 prototype that will be mounted on the carbon fiber structure, in which the carbon fiber is shorted to the bias filter ground through the 2 mm wide aluminum strip. Noise reduction by this proposed grounding scheme must be identified with the prototype module.

5.4 Hybrids

This section describes the hybrid design and related electrical issues for the stave design. The proposed beryllia hybrids minimize the amount of material in the detector and are a well-established technique used previously in a number of experiments.

Commonly, the circuits connecting the SVX chips to the low mass jumper cable are called "hybrids." The hybrids will be based on the technology of thick film deposition on ceramics successfully used in a number of high energy physics experiments including all CDF SVX detectors and the CLEO microvertex detector[27] . In our case, the 380 micron beryllia substrate will be used to reduce the amount of material in Layers 1 through 5 where the hybrids will be mounted directly in the sensitive volume. For Layer 0 which has off-board hybrids at higher Z, the material issue is of less importance. However, beryllia ceramic is preferred here because of its significantly better thermal conductivity with respect to alumina.

Thick film deposition by screen-printing is a mature technology allowing for a minimal via size in dielectric of 200 micron and minimum trace width of 100 micron. Multi-layer designs are routinely achievable. Typical thickness of dielectric and metal layers are 40 and 7 micron, respectively. We have identified CPT, Oceanside CA and Amitron, NH as our potential vendors. Both companies have solid backgrounds in hybrid production.

There are four types of hybrids in the proposed design. Two of them are 10-chip, double-ended versions for Layers 2 through 5: one for axial sensors (L2A hybrid) and one for stereo sensors (L2S hybrid). The others are a 6-chip, double-ended version for Layer 1 (L1 hybrid) and a 2-chip version for Layer 0 (L0 hybrid).

In addition to providing a secure mount for the SVX chips and cable connector, the hybrids also have capacitors for bypassing the analog and digital voltages and the detector bias. The low-mass flat cable connects to the hybrid with an AVX connector plug (hybrid side) and receptacle (cable side). These are 0.5mm pitch, low profile 50-pin connectors with a maximum height of 3.1 mm above the surface of the hybrid. The CDF Run IIa SVX detector uses similar connectors with a low failure rate. Placement of the connector on the hybrid allows for easy testing of hybrids with and without attached silicon sensors during all phases of the hybrid and stave production. This is essential for the modularity of the design and for quality checking during

[27] Nucl.Inst.Meth. **A435**, 9-15, 1999.

stave production. The extra material introduced by the connector is small and is crossed by particles only after two precise measurements in Layers 0 and 1.

The SVX control signals and readout bus lines are routed from the connector to the SVX4 chips via 100-micron wide traces. The traces stop near the back edge of each chip, where they transition into gold-plated bond pads. Aluminum wire bonds connect these pads to the bond pads on the chips. The chip power will be routed from the connector on a power plane, and there will be a dedicated ground plane in the hybrid. The total number of metal layers is 6.

Figure 115 shows the top metal layers of L1, L2A and L2S hybrids. As one can see, the layout of all these hybrids is very similar to each other. The dimensions of these hybrids are 45mm x 25mm for L1, 50mm x 41.9mm for L2A and 50mm x 43.8mm for L2S. The total hybrid thickness is specified to be smaller than 0.9 mm.

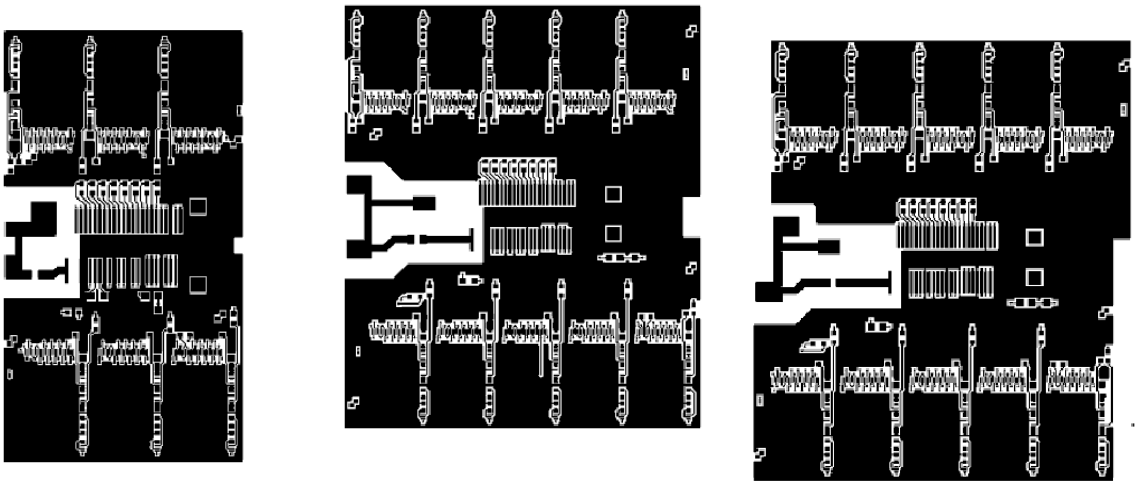
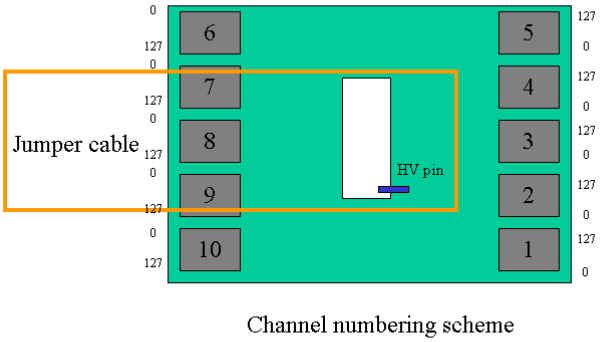


Figure 115. Top metal layer for L1 hybrid (left), L2A hybrid (center) and L2S hybrid (right)

Figure 116 specifies the adopted channel numbering scheme for 10-chip hybrids. The first chip to read out will be the chip in the corner closest to the HV pin on the connector. The readout then proceeds anti-clockwise with respect to the hybrid top side. The order of channels inside the chip is also shown. Six-chip L1 hybrids and two-chip L0 hybrids will be read out similarly.



Channel numbering scheme

Figure 116. Numbering scheme for 10-chip hybrid

We received 18 prototypes of the L1 hybrid from CPT in April 2002, and 23 prototypes of L2A hybrids from Amitron in July 2002. All CPT hybrids passed electrical tests for continuity and shorts. We found, however, one open trace on 4 Amitron hybrids. The flatness of the CPT hybrids was measured to be within the specification of 50 microns. The Amitron hybrids showed a considerable bowing, approximately a factor of 3 larger than the specification.

Figure 117 shows the prototype hybrids: top view of L2A hybrid from Amitron (left); L1 hybrid from CPT, top view (center) and bottom view (right). Notice that the L1 hybrid has no components or traces in the inter-chip area. This particular prototype has been developed under the assumption of a separate small board ("finger") placed between chips to provide all side bonding connections. This design is used by the CDF SVX detector in Run IIa. Later we abandoned this idea and found a way to integrate the finger into the hybrid, thus making overall design simpler. The L2A prototype has all necessary side components integrated in the layout. The back side of all hybrids will have a special printing to avoid glue in the area of the guard ring; see right photo in Figure 117. This should improve the breakdown voltage (hence, the radiation hardness) of the design, preventing potential discharge path through the glue in the region of the largest voltage difference between the edge of the detector and the first signal traces. The printing has two "pedestals" in the central area of the backside raising the hybrid above the guard rings of both sensors.

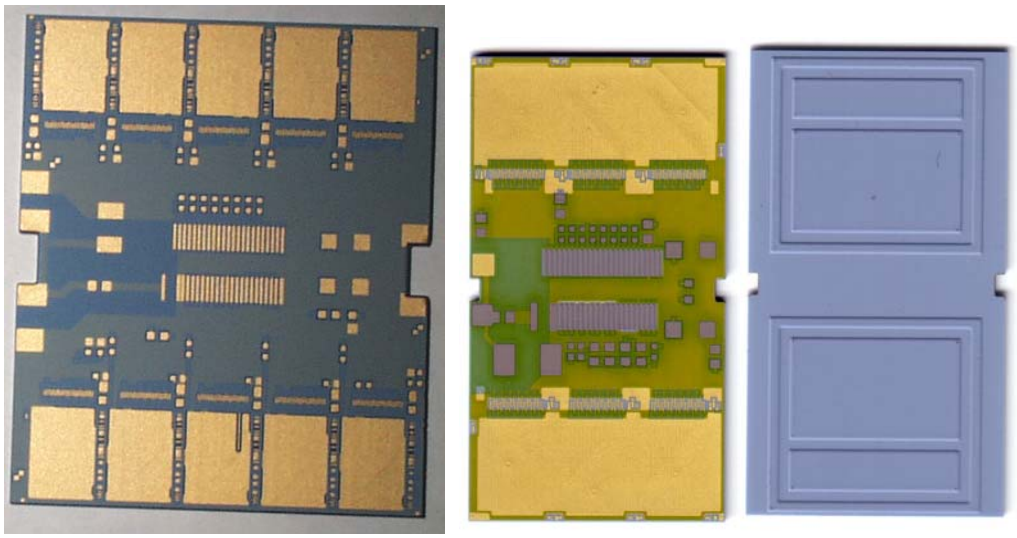


Figure 117.Prototype hybrids : Top view of L2A hybrid from Amitron (left); L1 hybrid from CPT, top view (center) and bottom view (right).

In July 2002 we assembled several L1 prototype hybrids (Figure 118). The prototype has 4 SVX4 chips at the corners of the hybrid. The two central chips were replaced by a simple finger kludge board to provide all side connections for two neighboring chips.

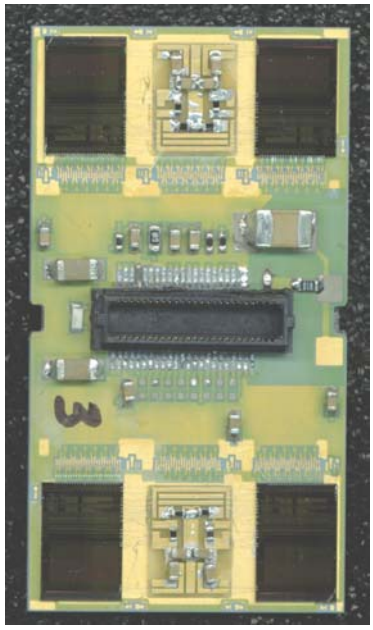


Figure 118. Prototype L1 hybrid

Using this hybrid and two prototype L1 sensors from ELMA we also assembled a L1 prototype module (Figure 119). Only two chips, #2 (bottom left) and #3 (bottom right) were bonded to sensors.

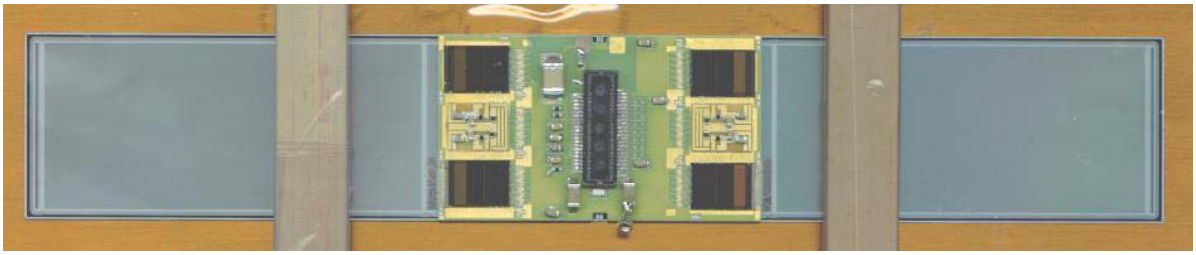


Figure 119. L1 prototype module

Figure 120 shows the channel ID, pedestal and total noise x 10 from readout of this L1 module. Noise is defined as the RMS of the pedestal. Four SVX4 chips are represented on the plot. The channel ID is incremented for each of them from 0 to 127. The value of pedestal was set at around 30 ADC counts. The noise level is approximately 1.0 ADC counts for chips 1 and 4, and 1.7 ADC counts for chips 2 and 3. The difference is explained by the extra capacitance load from the silicon sensors. The sensors were biased above depletion voltage at 50V. The total HV current for both sensors was 1.5 uA. Several noisy channels are visible for chips bonded to the detector. Making some assumptions about calibrations, we determine a preliminary noise of 700 e for bare chip and 1100 e for chips connected to silicon. This corresponds to a S/N of ~20:1 for the prototype module, assuming a MIP signal is 22000 e. Work is in progress to improve understanding of the noise level.

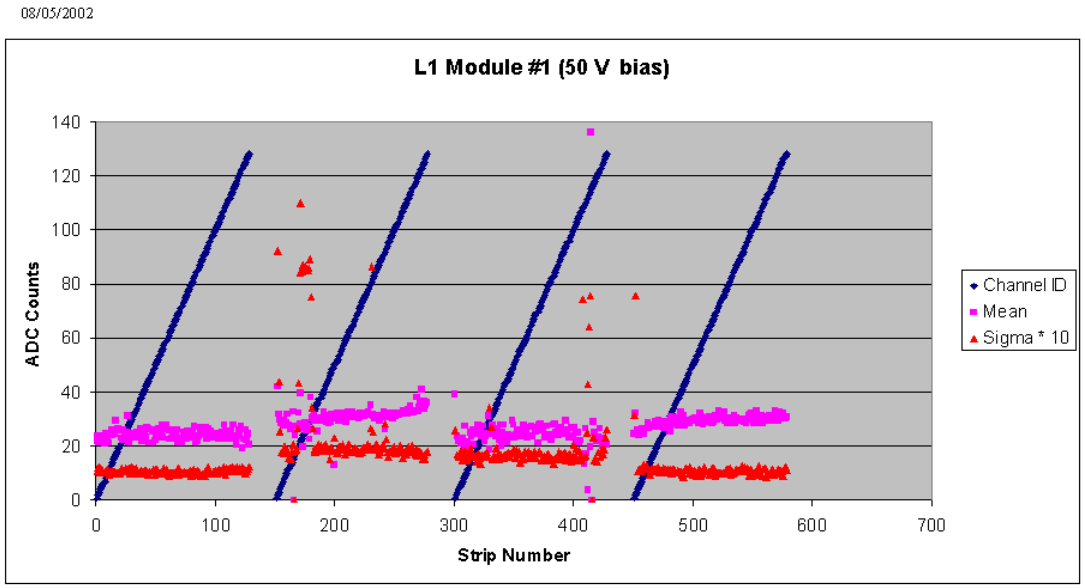


Figure 120. Channel ID, pedestal and noise plots for L1 prototype module

5.5 Cables, Adapter Card and Interface Board Overview

A primary goal of the Run IIB readout chain design is to preserve as much of the Run IIA electronics and cable plant as possible. In particular, we want to keep: 1) the Interface Boards (IBs), located at the base of the central calorimeter, that relay digital signals between the sequencers and the SVX4 chip, supply both low-voltage power and high-voltage bias, and monitor current and temperature; 2) the high-mass cables, consisting of 3M 80 conductor cables and parallel coaxial clock cables that run from the IBs to Adapter Cards on the calorimeter face. Because of the complexity of these IBs, any required changes beyond the scope of component replacements or hand-wired jumpers will likely mandate complete replacement. Also, the space for connectors on the IB face is saturated. A required line count into the IB exceeding that available on the 80-conductor cables could not be accommodated.

As described below, the present design aims to preserve the IBs by replacing the Run IIa passive Adapter Cards on the calorimeter face with active ones that translate between single-ended (IB) and differential (SVX4) signals, and that also regulate supply voltages. The long (up to 2.7 m) Run IIa low-mass cables, which do not have differential-signal capability, will be replaced with new cables comprised of Twisted Pairs connected by small, passive Junction Cards to new, relatively short, low-mass Digital Jumper Cables.

5.6 Digital Jumper Cables

Digital Jumper Cables (DJCs) will carry digital signals and power between the hybrids and the Junction Cards, where they connect to the Twisted-Pair Cables. In all, each DJC carries 11 pairs of differential signals, 6 single-ended signals, 5 sense lines, 2 power voltages and ground, and sensor bias of up to 1000 V. They will be flex-circuit striplines similar to the low-mass cables used in Run IIA, which minimize the amount of material in the sensitive volume. Although they will be shorter than the Run IIA cables, they will be narrower and carry more signal traces, so that the feature size is 20% smaller. There will be 888 DJC's 14.7 mm wide, with a distribution of lengths between 44 cm and 103 cm. Signal traces 125 microns wide with 300 micron pitch, and also broad power and ground traces, will be located on both sides of a Kapton dielectric 102 microns thick. The layout for all five layers is the same, with a 50-pin, 0.5 mm pitch AVX 5046 connector soldered to pads on both ends. DJC's for Layers 2-5 will be made with 1-ounce rather than ½-ounce copper traces because of their larger (10-chip) power requirements. The DJC's will be reinforced by thin G10 backing behind the connectors to make them more robust during handling. Photographs of one end of a 50 cm prototype DJC (before connector installation) are shown in Figure 121 and Figure 122.

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Figure 121. Digital jumper prototype cable: side opposite the connector

Figure 122. Digital jumper prototype cable : connector side

The prototyping program aims to qualify at least two vendors as well as to validate the design. As of 30 August 2002, one vendor (Honeywell FM&T) has successfully produced both 50 cm and 100 cm prototypes, while a second (Basic Electronics, Inc.) has produced 50 cm cables and is now working on the 100 cm version.

A hybrid stuffed with four SVX4 chips has been successfully read out with a 50 cm DJC. In addition, thirty 50-cm prototypes have so far been bench-tested, both singly and daisy-chained to make a 100 cm cable. The results are: 1) only a few fabrication defects have been found, all of them bad solder joints at the connectors; 2) the high-voltage trace gives no problems, even at several hundred volts above the required 1000 V; 3) signal quality after 100 cm is good; 4) measured impedances (107 ohms for differential lines, 61 ohms for single-ended lines) are close to design values; 5) cross-talk is negligible for differential lines and acceptable (≤13%) for single-ended lines.

5.7 Junction Cards

Junction Cards are impedance-controlled passive boards that mate Digital Jumper Cables with the Twisted-Pair Cables that run to the Adapter Cards. They will be mounted near the present location of the Run IIA H-disks, and will have a maximum size of 25x90 mm^2. Junction Cards must be mechanically robust and securely mounted. All attached cabling will be stress-relieved whenever possible. The Twisted-Pair Cables will be soldered to one end of the cards for increased strength, while the Digital Jumper Cables will plug into 50-pin AVX 5046 connectors. Junction Cards for Layers 0 and 1 will each join three pairs of cables, while those for Layers 2 – 5 will each join two pairs. Bypass capacitors to smooth the supply voltages will also be located on the Junction Cards because there is limited space for large capacitors on the hybrids.

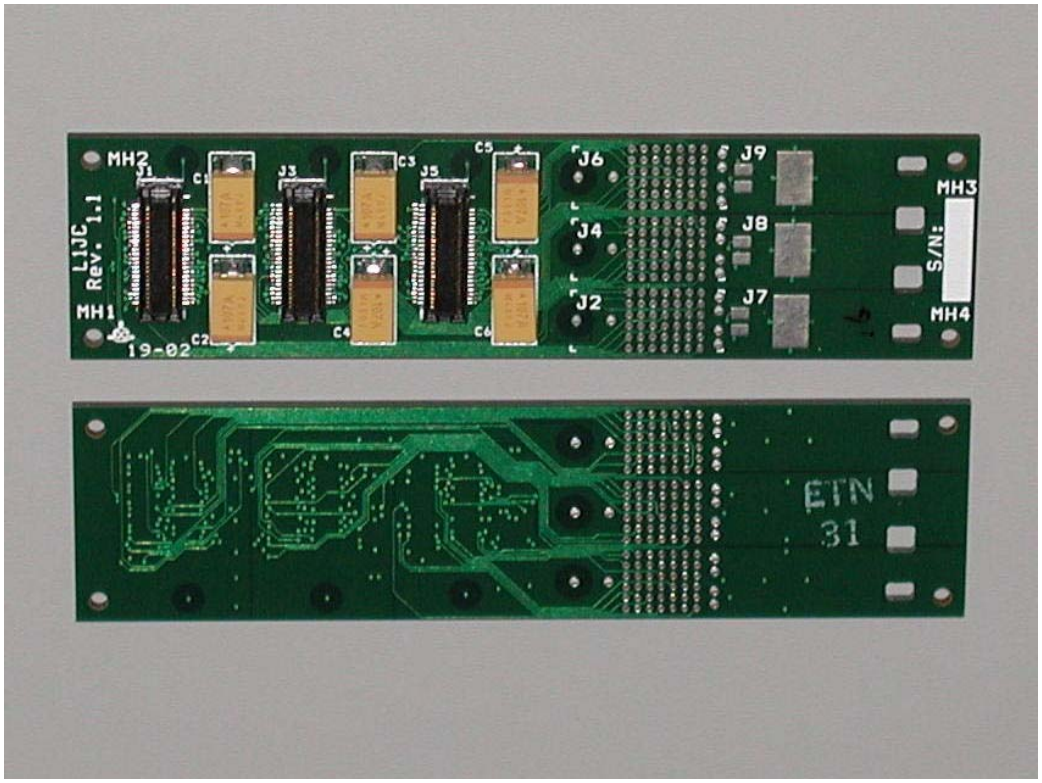


Figure 123. Prototype junction card

As of 30 August 2002, prototypes for the L0-1 Junction Cards were in hand, and the schematic for the L2-5 version is complete. Figure 123 is a photograph of a prototype Junction Card.

5.8 Twisted Pair Cable

The Twisted Pair Cable, approximately 2 meters long, connects the Junction Cards and Adapter Cards. The cable is soldered to the Junction Card on one side and is terminated by connectors on the Adapter Card side. The cable mass is not a major issue because the cable is outside of the tracking volume. The total outer diameter of a Twisted Pair bundle can be as small as 5-6 mm.

The twisted pairs were chosen because 11 of the signals used by the SVX4 chip are differential. The 5 slower single ended lines will also use twisted pairs. The cable assembly has 2 power lines and their returns, 1 HV line and its return, 15 signal twisted pairs, one temperature sensor twisted pair and 2 voltage sensor pairs. The clock signals are transmitted via two coaxial cables in the same assembly. Two versions of the Twisted Pair Cable are envisioned (Layers 0-1, Layers 2-5) depending on the HV and power requirements.

Figure 124 specifies connections between junction card and adapter card.

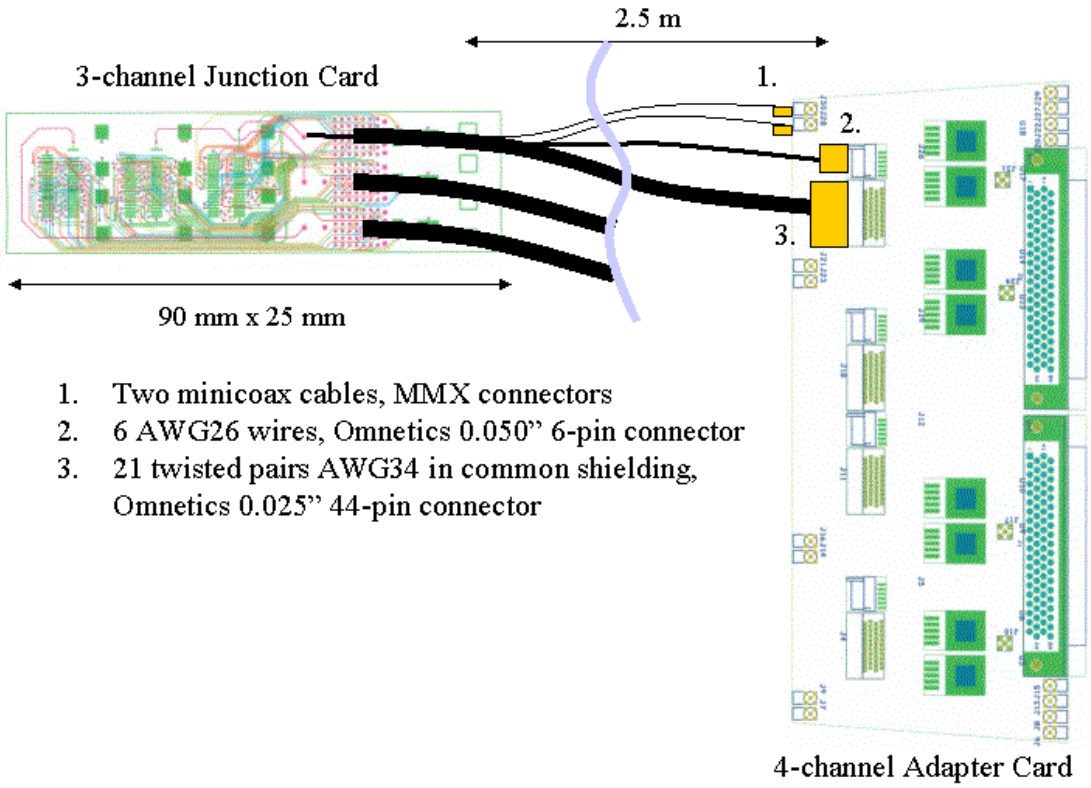


Figure 124. Schematic connection between junction card and adapter card

Figure 125 shows prototype cables for the twisted pair cable assembly; from left to right : two connectors for micro-coax cables, 44-pin Omnetics connector for signal pairs, 6-pin Omnetics connector for HV and power lines. The signal twisted pair was produced by New England Wire and was terminated to the connector by Omnetics.

Figure 125. Prototype cables for the twisted pair assembly; from left to right : two connectors for micro-coax cables, 44-pin Omnetics connector for signal pairs, 6-pin Omnetics connector for HV and power lines.

5.9 Adapter Card

For Run IIB, new active Adapter Cards will replace the passive cards now mounted on large "horseshoes" on the north and south faces of the calorimeter. They will 1) translate single-ended TTL logic signals from the Interface Cards to differential signals to and from the SVX4 chips; 2) regenerate clock signals; 3) regulate the two 2.5 volt SVX4 supply lines to within the narrow 250 mV tolerances of the SVX4. To use the limited mounting space more efficiently, each Adapter Card will service four or six channels rather than the two channels of Run IIA. Each pair of channels requires an 80-pin mini-D connector and four miniature coax connectors to interface with the High Mass Cables and associated clock coax cables, and two fine-pitch connectors on the Twisted-Pair side. Additional connectors are required for powering the adapter board itself, and for strobing lines.

Suitable components have been found and tested for signal translation and refreshing, and a voltage-sensing regulator circuit that will use sense lines in the Twisted Pair and Digital Jumper Cables has been successfully bench-tested. Layout of the prototype boards is complete (Figure 126), and three have been fabricated and tested. The largest remaining issue is how to remove the heat, about 600 watts on each calorimeter face. Heat sinks must be designed to transfer heat

effectively from Adapter Card components to the horseshoe mounting plates, and the horseshoes themselves must be cooled.

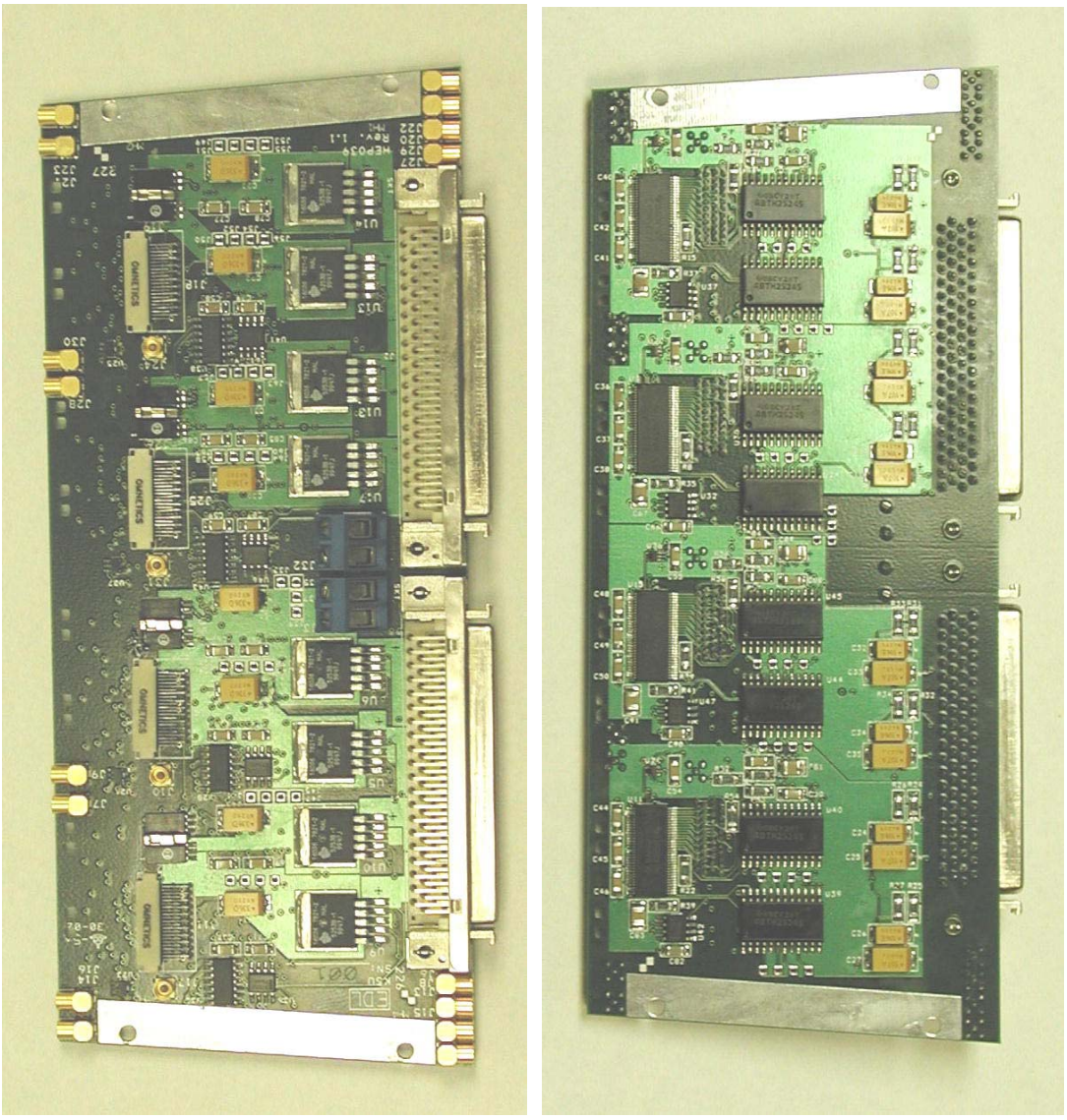


Figure 126. Top and bottom sides of a prototype adapter card

5.9.1 Adapter Card Implementation Details

Table 21 - Preliminary adapter card input connector (80 conductor cable from interface board).

Pin #	Function	Pin #	Function
1	Secondary Bias A	41	NC
2	GND	42	NC
3	GND	43	Primary Bias A
4	GND	44	3.3 V
5	Temperature A	45	3.3 V
6	VCAL A	46	3.3 V
7	D7 A	47	3.3 V
8	D6 A	48	2.5 V Unregulated AVDD A
9	D5 A	49	2.5 V Unregulated AVDD A
10	D4 A	50	2.5 V Unregulated AVDD A
11	D3 A	51	2.5 V Unregulated AVDD A
12	D2 A	52	2.5 V Unregulated AVDD A
13	D1 A	53	2.5 V Unregulated AVDD A
14	D0 A	54	2.5 V Unregulated AVDD A
15	Priority In A	55	2.5 V Unregulated DVDD A
16	Mode 0 A	56	2.5 V Unregualted DVDD A
17	Mode 1 A	57	2.5 V Unregulated DVDD A
18	Change Mode A	58	2.5 V Unregulated DVDD A
19	DValid A	59	2.5 V Unregulated DVDD A
20	Priority Out A	60	2.5 V Unregulated DVDD A
21	GND	61	3.3 V
22	Temperature B	62	3.3 V
23	VCAL B	63	3.3 V
24	D7B	64	3.3 V
25	D6 B	65	2.5 V Unregulated AVDD B
26	D5 B	66	2.5 V Unregulated AVDD B
27	D4 B	67	2.5 V Unregulated AVDD B
28	D3 B	68	2.5 V Unregulated AVDD B
29	D2 B	69	2.5 V Unregulated AVDD B
30	D1 B	70	2.5 V Unregulated AVDD B
31	D0 B	71	2.5 V Unregulated AVDD B
32	Priority In B	72	2.5 V Unregulated DVDD B
33	Mode 0 B	73	2.5 V Unregulated DVDD B
34	Mode 1 B	74	2.5 V Unregulated DVDD B
35	Change Mode B	75	2.5 V Unregulated DVDD B
36	DValid B	76	2.5 V Unregulated DVDD B
37	Priority Out B	77	2.5 V Unregulated DVDD B
38	Primary Bias B	78	GND
39	NC	79	GND
40	NC	80	Secondary Bias B

Table 22 - Preliminary adapter card output connector pinout.

Pin #	Function	Pin #	Function
1	Primary Bias	21	D2+
2	Secondary Bias	22	D2-
3	AVDD	23	D1+
4	GND	24	D1-
5	Sense A +	25	D0+
6	Sense A -	26	D0-
7	Temperature	27	DV+
8	Temperature Return	28	DV-
9	VCAL	29	Priority Out +
10	NC	30	Priority Out -
11	D7+	31	Clock +
12	D7-	32	Clock -
13	D6+	33	Mode 0
14	D6-	34	Mode 1
15	D5+	35	Change Mode
16	D5-	36	Priority In
17	D4+	37	Sense D +
18	D4-	38	Sense D -
19	D3+	39	GND
20	D3-	40	DVDD

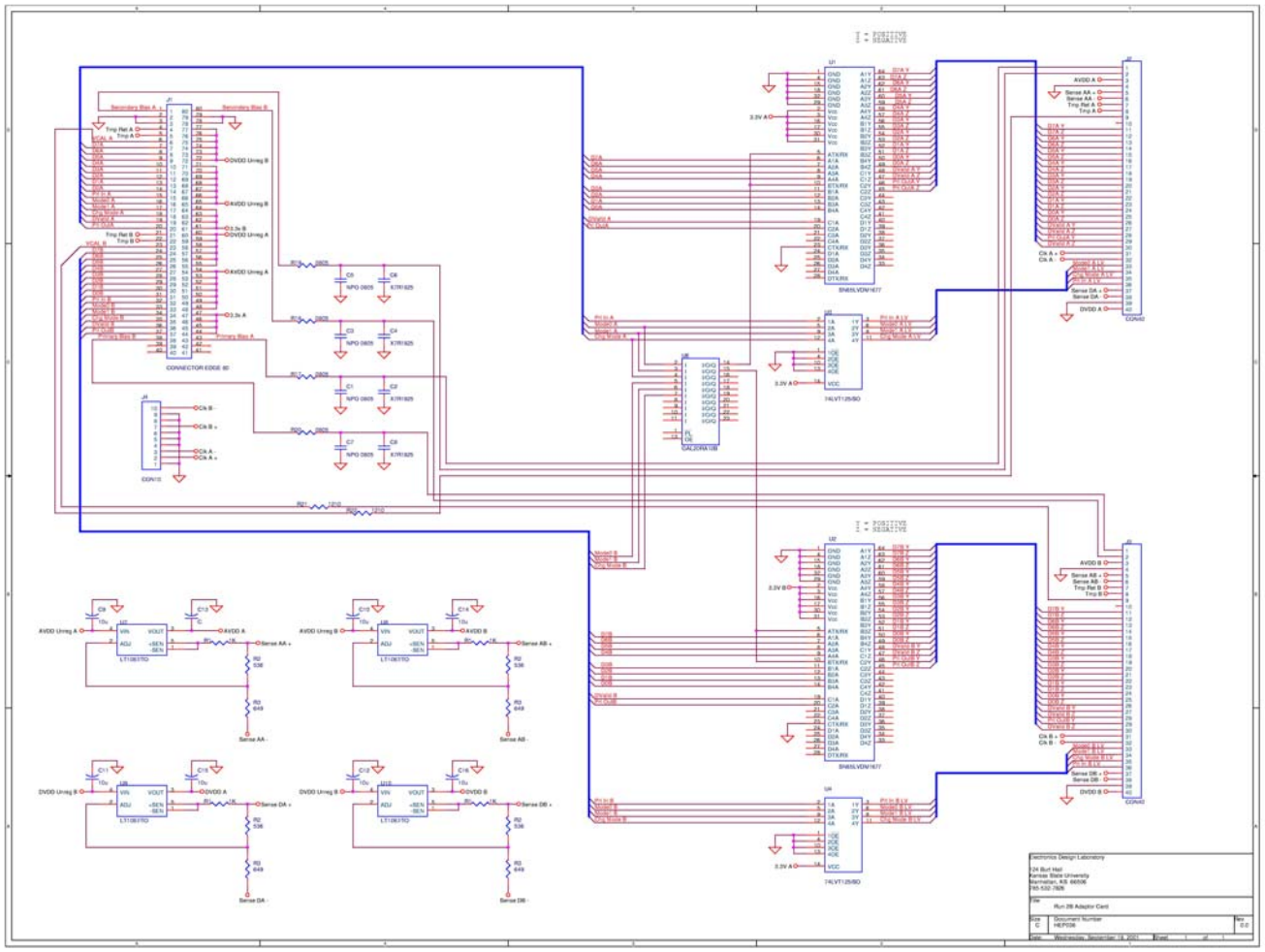


Figure 127 - Preliminary schematic for the adapter card.

5.9.2 Purple Card

A variant of the Adapter Card, called the “Purple Card”, will be used in test stands for testing and burn-in of hybrids and sensors. The Purple Cards combine the functions of the Adapter Cards and Twisted-Pair Cables, and some functions of the Interface Boards, in these simplified test stands; they serve as an interface between the same Stand-Alone Sequencers used in the Run IIA test stands and Digital Jumper Cables. Engineering information gleaned from early use of the Purple Cards will be applied to improve the Adapter Card design. As of 30 August 2002, six Purple Cards have been built, and a Purple Card has successfully read out a 4-chip hybrid. A second iteration on this card is underway, incorporating modest design and layout revisions motivated by SVX4 testing. Figure 128 shows a prototype Purple Card.

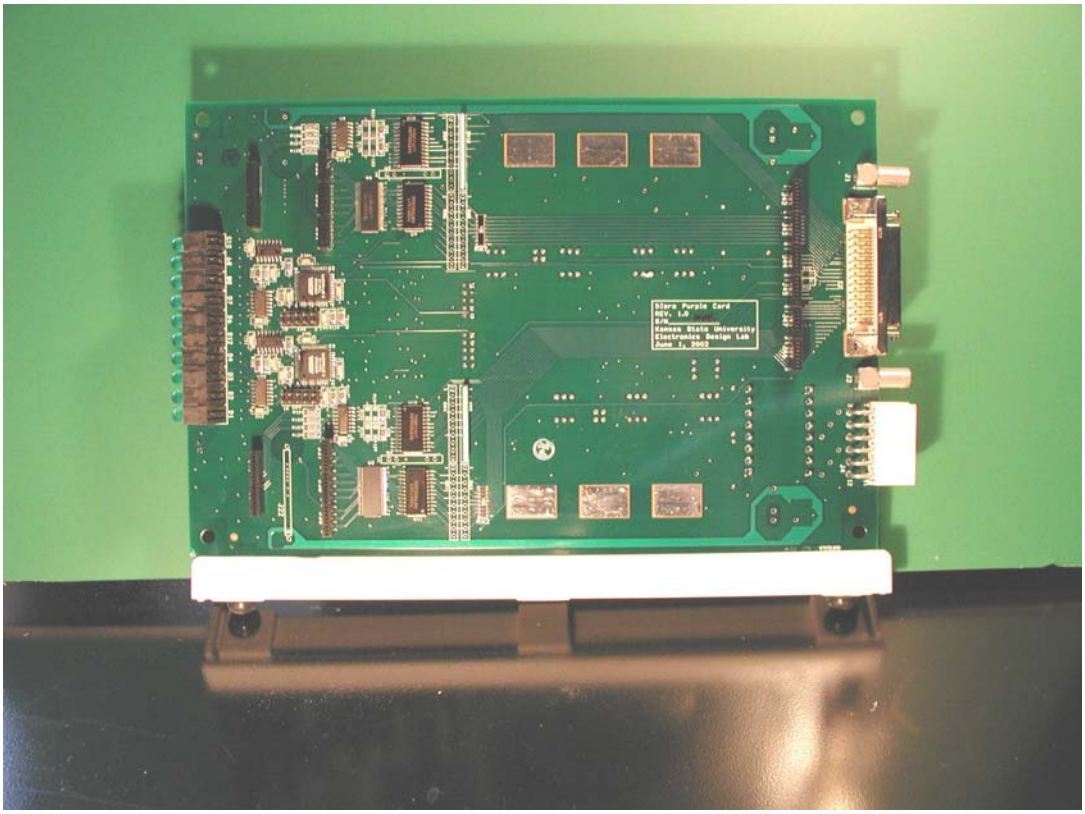


Figure 128. View of a prototype Purple Card

5.10 Interface Board

In order to avoid the considerable expense of designing and building new Interface Boards (IB), the existing IBs must be recycled. All new features for Run IIb are incorporated into the active Adapter Card. The IB detector bias distribution was tested to + 200 V, -100 V (including the switching relay) and should be safe for 300 V for silicon Layers 2-5. Bias cables for Layers 0-1 (up to 1000 V) cannot go through either the IB's or the existing high-mass cables, but will be routed separately.

Required changes on the IB which have been identified to date include: 1) replacing data line terminations (24 resistor changes per channel); 2) probable changes in control line termination, and in the clock equalizer circuit; 3) new set points for current and temperature trips; 4) reprogramming of 5 PLDs; 6) changes to priority-out signal threshold and hysteresis (this line was underdriven by the SVX2 chip). The total number of changes is about 200 per IB.

5.11 Sequencer

The firmware in the sequencer needs to be adjusted for the difference between the SVX4 chip operating in the SVX2 mode and real SVX2 chip. The changes are rather straightforward and imply remapping of the SVX2 lines to SVX4 lines. The required remapping was shown in the section describing the SVX4 chip.

5.12 Low Voltage Distribution

Currently VICOR switching power supplies [28] are used to provide power for the SVX2 chips and Interface Boards. For Run IIb we intend to preserve those supplies and the distribution scheme through the Interface Boards.

The massive power lines from the VICOR supplies are split between different channels in the fuse panel. After the individual protection fuses, the power is distributed to the custom J1 backplane of 9U x 280 mm custom crates. The J2 and J3 backplanes of the crates provide connectors for the cable runs to the sequencers, while J1 contains connectors for low-voltage power for each Interface Board and up to eight dependent silicon hybrids, the 1553 connector and bus (used to monitor the SVX4 power and current, and hybrid temperature), and a connector to bring in 16 bias voltages and returns for eight hybrids.

We are investigating the feasibility of replacing the J1 backplane. This would have the benefit of eliminating the existing fuse panels; these panels are time-consuming to wire, and contain ~150 fuses which experience has shown to be somewhat unreliable due to oxidation of contacts. A small number of fuses would still need to be placed for safety reasons on J1 and perhaps on the IB (replacing existing ferrite beads there). Another advantage of J1 replacement is that remote sensing from the external power supplies would go to the J1 bus instead of stopping at the fuse panel. We will have more space at the backplane because a 34-pin bias connector can be replaced with a smaller one, since the new single sided detectors only need one bias voltage. The feasibility of this scheme must be established, and mechanical and electrical layouts need to be done. The Interface Board side of the backplane would be unchanged.

5.13 High Voltage Distribution

Reliable high voltage operation is crucial to ensure the increased radiation tolerance of the new Silicon Tracker. Operation at voltages up to +1000 V is specified for the Layers 0 and 1 and up to +300 V for the Layers 2 through 5.

The high voltage bias will be applied to the backplane of the single-sided silicon sensors. For 10-chip hybrids the high voltage will arrive at the hybrid on the Jumper Cable and will be routed to a side pin of the AVX connector. Two neighboring pins will be removed to ensure a safe distance to the nearest ground. The proposed scheme has been tested to operate reliably to 2 kV with a prototype jumper cable and a stuffed L1 prototype hybrid. The bias voltage will be brought to the sensor backplane with a foil wrapped around the sensor edge and glued to the backplane with a conductive silver epoxy. The foil will be insulated from the sensor edge and from the outside with a 50 micron Kapton tape. For Layer 1 the backplane connection will be provided similarly to the 10-chip hybrids while for Layer 0 the bias voltage will be fed to a line on the analog cable and then will be connected to the backplane of the sensor near the end of the cable.

[28] 4 kw MegaPAC AC-DC Switcher, Vicor Corporation, Andover, MA.

Despite the fact that Run IIa silicon detectors require operating bias voltages only within ±100 V, the specifications of the existing Run IIa HV power supplies are adequate for Run IIb detectors. Software compatibility and reliable operation of the current system during the first year of Run IIa are two other important considerations. Therefore, the most straightforward upgrade path for the HV system will be to keep the existing Run IIa system increasing the number of channels as needed.

For all layers one HV line is used per hybrid. Therefore, each sensor in Layer 0, two sensors in Layer 1 and two or four sensors in Layers 2-5 will share the same HV line. The total number of HV lines is 888 corresponding to the total number of hybrids. A possibility of bias splitting between two or more hybrids in the outer layers should be considered to reduce the number of HV channels. The table below shows HV currents per strip, per hybrid and per stave calculated for sensors irradiated by equivalent of 15 inverse fb. For layers 2-4 the 20 cm long sensor gangs were considered for calculation of current per hybrid.

Table 23. HV currents per strip, per hybrid and per stave for Layers 0-4

Layer	Radius,m	uA/strip	uA/hybrid	uA/stave
0	18	1.2	310	NA
1	35	0.46	360	NA
2	54	0.28	530 max	1790
3	86	0.12	230 max	770
4	116	0.06	180 max	550

Based on the above information the proposed splitting of the HV channels is the following:

- One HV channel per hybrid for layers 0,1 and 2
- One HV channel per two hybrids for layer 3
- One HV channel per stave (i.e. four hybrids) for layers 4 and 5

The splitting equalizes currents for HV channels servicing different layers. The total number of required HV channels in the proposed scheme is 492.

In the Run IIa system, bias voltages are supplied from a BiRa VME 4877PS High Voltage Power Supply System[29]. The system utilizes the three HVS power supply types shown in Table 24.

[29] Model VME 4877PS High Voltage Power Supply System Manual, March 1988, Bi Ra Systems, Albuquerque, NM.

Over-voltage protection is provided through trim potentiometers located on the front panel of the modules.

Table 24 - HVS power supply types used in the DØ Run IIa silicon bias voltage system.

HVS type	max output voltage, kV	max output current, mA	number of channels
HVS5.5P-1	+5.5	2.3	116
HVS5.5N-1	-5.5	2.3	152
HVS2P	+2.0	3.2	116

Each of the ten VME crates in the Run IIa HV system holds a Power PC controller and six motherboards containing eight Bi Ra power supplies each. Power to the VME crates is delivered from Lambda power supplies. Run IIb system with 492 HV channels will require 62 motherboards, as well as 11 VME crates with controllers and power supplies. It is prudent to assume some amount of spare channels so we plan to populate all 66 slots in 11 crates with motherboards that will increase the total channel count to 528. In terms of infrastructure this will not be a big change since the current SMT HV system is already using 10 VME crates. However, the number of positive HV pods will need to be increased considerably.

The Run IIa fanout and breakout boxes will need a replacement. The fanout boxes are used to split HV channels between different HDIs and to provide hardware protection against accidental application of HV higher than 150 V. The breakout boxes are used to distribute HV to the Interface Boards and to transfer temperature signals from the Interface Boards to interlock control systems. For Run IIb design we plan to combine the fanout and breakout boxes and move the temperature control functionality to a separate system.

It has been checked that the HV path through the Interface Board and 80-conductor cables can sustain up to 300 V and, therefore, can be preserved in Run IIb for Layer 2-5 bias distribution. The design goal for HV distribution for the inner two Layers is operation at 1000 V. In this case, the HV cabling needs to bypass the Interface Board and go directly to the Adapter Card via a separate cable.

5.14 Performance

Increased luminosity in Run IIb will result in high occupancy in the detector especially for the inner layers. This has several implications for the readout performance. Two areas of concern, the SVX4 dynamic range and the detector readout time, were addressed in our simulations with results presented in this Section.

The charge-sensitive preamplifier of the SVX4 chip integrates incoming signals and, therefore, needs to be reset regularly to prevent saturation. The saturated preamplifier will result in

inefficiency of the detector. The reset time in SVX4 is equal to several hundred nano-seconds. Usually the resets are performed during the Tevatron abort gaps, which are periods of time within one revolution without collisions. Along with other modifications the high luminosity regime of the Tevatron operation in Run IIb will include reduction of the available abort gaps to possibly one per revolution. The current 36 bunches x 36 bunches operation allows for 3 abort gaps per revolution.

The full GEANT simulation with the Run IIb geometry discussed in Section 8.5, and realistic clustering in the silicon has been used to estimate charge accumulated per strip after 450 minimum bias events. A scenario of 150 beam crossings before a reset with 3 minimum bias interactions per beam crossing was assumed. Figure 129 shows the charge per strip in the innermost layer after 450 minimum bias events. The left plot corresponds to the sensors in the central (closest to z=0) barrels. The right plot corresponds to the sensors in the end barrels. The central sensors are crossed by a larger number of particles while the incidence angles are shallower for the end sensors allowing for a larger deposited charge. As shown by arrows in both cases about 1% of strips will receive charge in excess of approximately 100 fC, which corresponds to 25 minimum ionizing particles. The dynamic range of the SVX4 chip was chosen to be 200 fC, leaving some margin for high luminosity operation. The expected inefficiency caused by the preamplifier saturation is expected to be less than 0.1%.

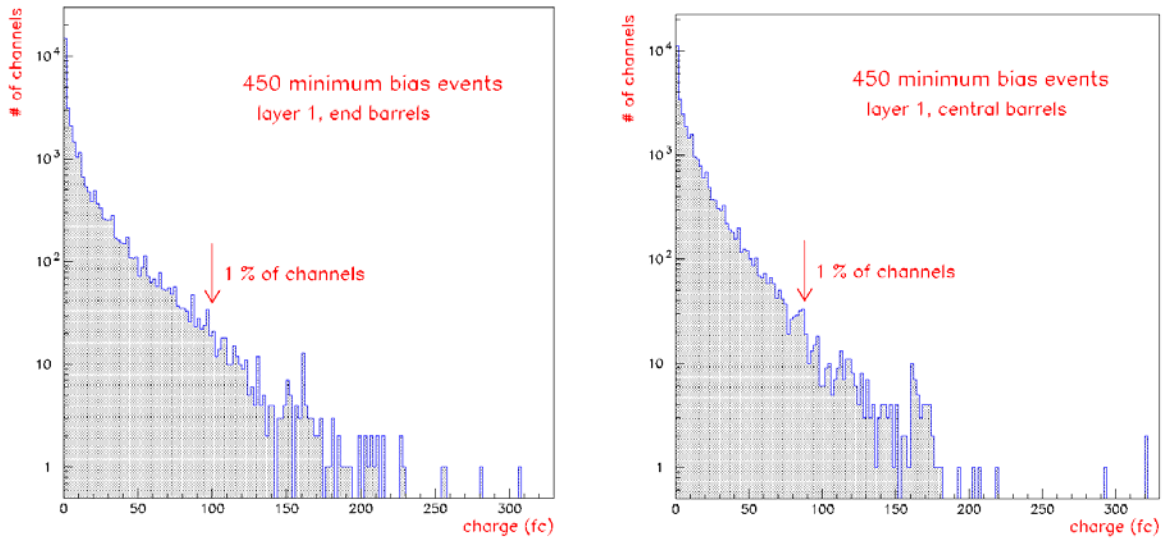


Figure 129 - Charge per strip in the innermost layer (labeled layer 1 in the figure) after 450 minimum bias events. The left plot corresponds to the sensors in the central, closest to z=0, barrels. The right plot corresponds to the sensors in the end barrels.

Another important performance issue for data acquisition is the readout time. A p-pbar interaction triggered for readout will be accompanied by several minimum bias interactions. To investigate a wider range of Level 1 triggers, several simulated samples were used: minimum bias, two jet and WH events. The maximum number of strips per readout cable in a layer was determined for each event. This number corresponds to the slowest chain of readout in this layer

and is relevant to estimate the readout time for the detector and the associated dead time. The number of hit strips has been scaled by appropriate factors to account for the closest neighbors that normally are also included in the sparse mode readout. The factors were determined from the cluster size distributions and were typically around 1.7 for the cases without noise and 2.8 for the cases with noise. Figure 130 shows the maximum number of strips per readout cable as a function of radius for minimum bias events (left plot) and QCD two jet events (right plot). Each layer corresponds to two points in those plots from different sublayers. Four different cases were considered: without noise for the two thresholds of 4 and 5 ADC counts, and with noise (rms 2.1 ADC counts) for the same thresholds. The average simulated signal was equal to 20 ADC counts corresponding to a S/N ratio of 9.5. Figure 131 shows the maximum number of strips per readout cable as a function of radius for WH + 0 minimum bias events (left plot) and WH + six minimum bias events (right plot).

Comparison of the inner three layers with the highest rates suggests that Layer 1 with 6 chips in the readout chain and Layer 2 with 10 chips will operate in similar conditions for all types of events. Layer 0 with 2 chips in the readout chain has rates a factor of 2 lower. However, this layer will experience the worst radiation damage and, as a result, a lower S/N. The effect of the noise on occupancy depends on the threshold. For the threshold over noise ratio equal to 2.4 the deterioration of S/N from 9.5 to 8 increases the maximum number of readout strips by 40% in Layer 0, by 50% in Layer 1 and by 75% in Layer 2, all for two jet events. The largest increase is observed in the 10-chip readout chain of Layer 2 due to the simple fact that the number of noisy strips is proportional to the number of chips. A lower S/N ratio in the innermost layer 0 can easily increase the number of readout strips by a factor of two and make its rate comparable to the Layers 1 and 2. As a result of these simulations, we feel it is prudent to daisy-chain only two chips in Layer 0 and leave a safety margin to accommodate higher noise occupancy in this layer after irradiation.

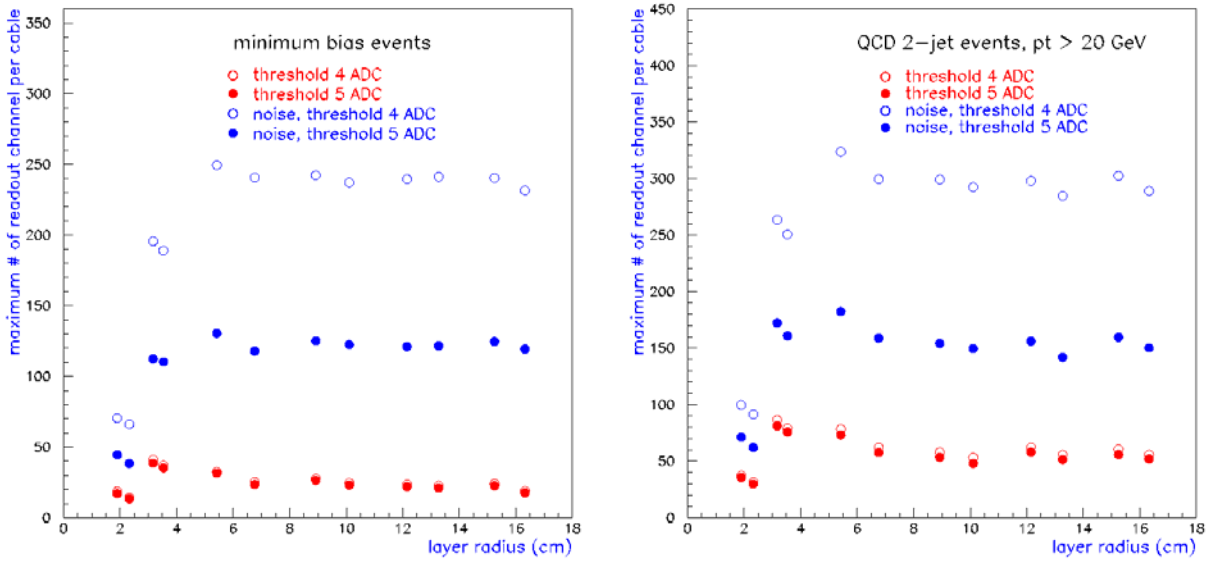


Figure 130 - Maximum number of strips per readout cable as function of radius for minimum bias events and QCD two jet events

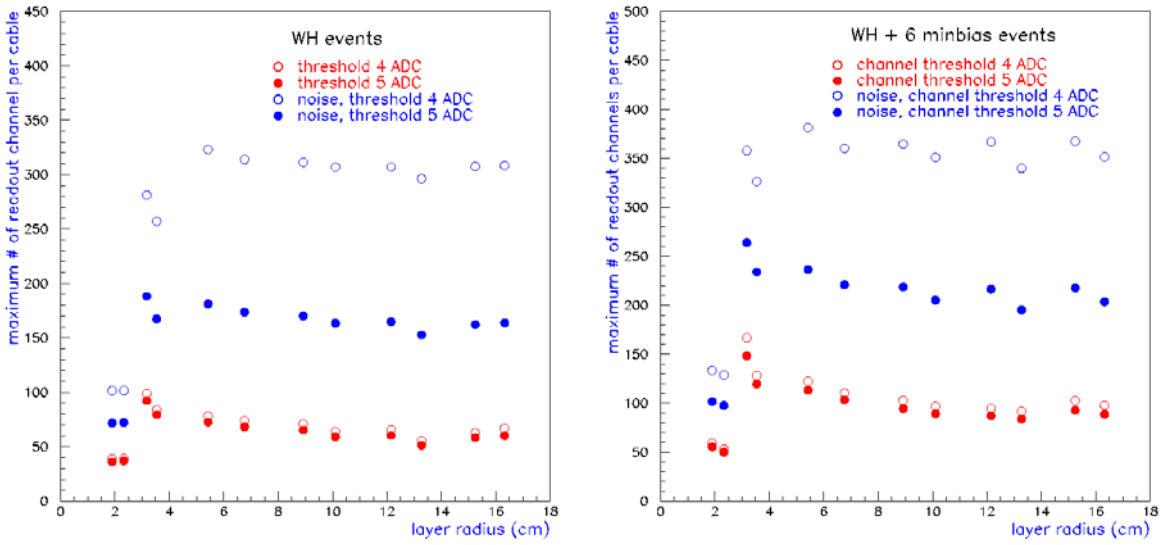


Figure 131 - Maximum number of strips per readout cable as function of radius for WH + 0 minimum bias events and WH + 6 minimum bias events.

The above information is useful for the evaluation of the deadtime. The readout of SVX4 is driven by a 53 MHz clock. Two bytes of data per channel (address and amplitude) require two clock cycles. This gives a total readout time of an SVX4 chip of about 4 microseconds for a typical occupancy of 100 strips. The deadtime will be determined by the SVX4 digitization time, readout time and the pipeline reset time after the readout. Though the correct calculation

should combine information from all silicon layers and all levels of the DØ trigger in a queue analysis, essentially one buffer structure of the DØ data acquisition makes a simple rough estimate possible. The total deadtime can be estimated as

3 (digitization) + 4 (readout) + 4.2 (pipeline reset) = 11.2 microseconds

At 10 kHz Level2 trigger input rate, corresponding to 100 microseconds between Level_1_Accept signals, the deadtime will be equal to approximately 11.2%. The deadtime and the readout time are acceptable for the DØ data acquisition system and in particular for the Silicon Track Trigger at Level 2.

5.15 Carbon Fiber Grounding Studies

A significant concern in the electronic and mechanical design of the detector is the proper grounding of carbon fiber elements. Highly conductive carbon fiber will be used for the cooling tubes and mechanical support structures. These carbon fiber elements have the potential to exhibit strong capacitive coupling to the sensors The experience of CDF in Run IIa with L00 cooling tubes has shown that sensor coupling to nearby floating metal can be a very troublesome source of noise. It is imperative that all carbon fiber in the detector is effectively shorted to the hybrid (L1-L5) or bias filter (L0) grounds to prevent capacitive noise transmission to the sensor readout.

The first test on the carbon fiber was to verify its conductivity through capacitive coupling. Two identically sized plate capacitors were constructed: the first with one copper plate and one type K139 carbon fiber plate, the second with two copper plates. Both capacitors were measured to be 132±2 pF. Additionally, each capacitor was individually connected in series to a network analyzer to produce a high-pass filter. The transfer functions and break frequencies for the two capacitors were identical. Therefore, the conductivity of the K139 carbon fiber is high enough to make it virtually indistinguishable from copper in terms of capacitive noise transmission. Furthermore, K139 is the carbon fiber type that will be used in L2-L5. K13C, which is more conductive than K139, will be used in L0-L1where the proximity of sensors to carbon fiber is much greater.

Because the grounding concerns are most acute in L0, a test was conducted to determine the feasibility of shorting a prototype L0 K13C carbon fiber cylinder to a hybrid or filter ground plane. The test configuration is shown in Figure 132. The interior of the castellated L0 cylinder was driven with the source power from the network analyzer. A sensor/filter mockup constructed of aluminum and Kapton layers was mounted on the cylinder with the network analyzer input wired to the sensor aluminum layer, and both the source and input grounds wired to the filter plane. Transfer functions to the sensor were measured with different configurations for shorting the carbon fiber to the filter plane. One to four 1/8” wide strips of 1 μm thick aluminized Mylar, 0.5 mil aluminum, or copper tape were attached across the filter and carbon fiber. The effectiveness of the grounding strips was tested with and without additional cooper tape coupling to the carbon fiber. The aluminized Mylar strips were minimally effective in reducing power to the sensor. Aluminum and copper strips performed equally well. The power

reduction was independent of the number of strips, but proportional to the amount of copper tape used to couple the strips to the carbon fiber, up to a maximum reduction of 40 dB at 1 MHz.

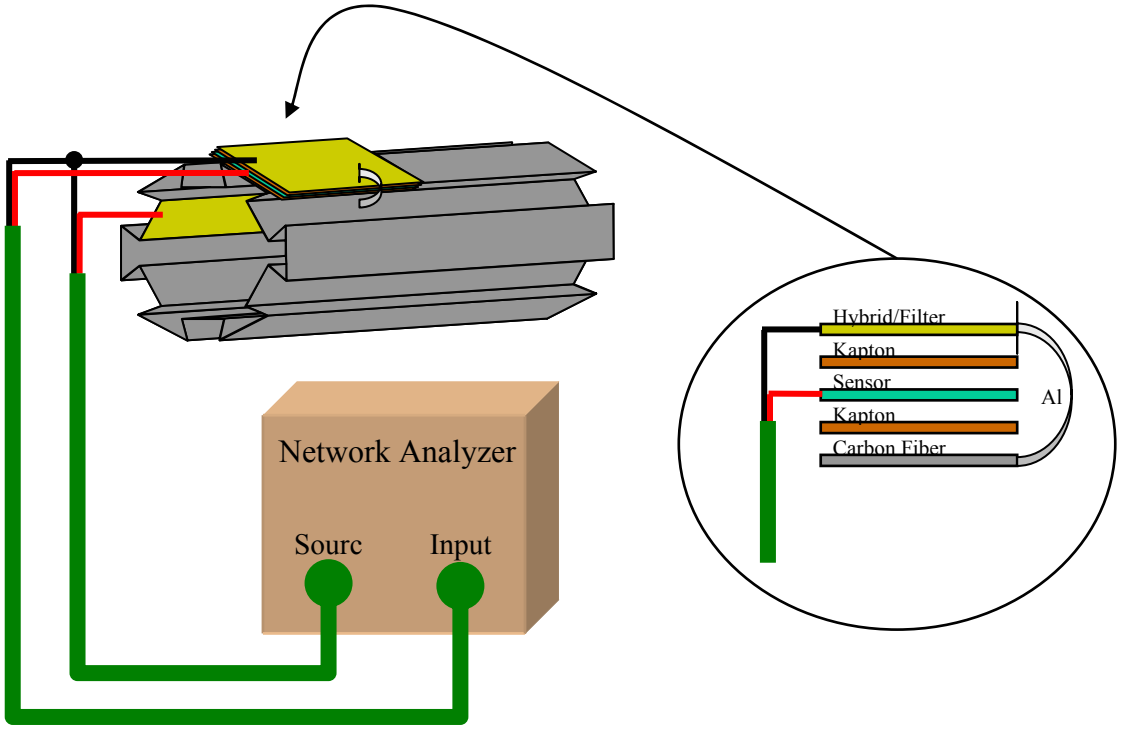


Figure 132. L0 Grounding test setup.

A more systematic test of the relation of attenuation to the coupling area to carbon fiber was performed using a 36 in^2 parallel plate copper-carbon fiber capacitor. Figure 133 shows that increasing the area of copper tape coupling to the capacitor dramatically increased the attenuation up to a saturation point of about 4 in^2.

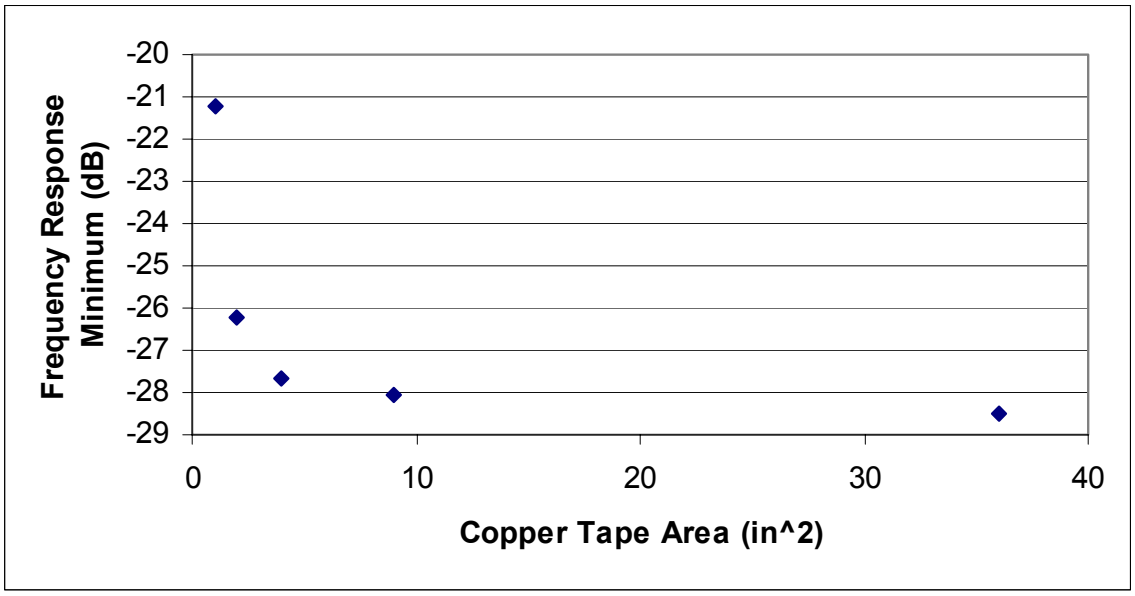


Figure 133. Attenuation at 74 MHz as a function of coupling contact area.

Because copper tape coupling would be unfeasible in the detector, a coupling test was carried out using carbon fiber pieces with embedded aluminum foil and aluminized Mylar. A new sensor/hybrid mockup was built and mounted on different pieces of K13C carbon fiber with various amounts of surface area covered with embedded aluminum. The embedded aluminum extends out to grounding strips that fold over and attach to the hybrid/filter plane. A diagram of this setup is given in Figure 134. The coupling point on the actual planes will be 2 mm wide ground pads.

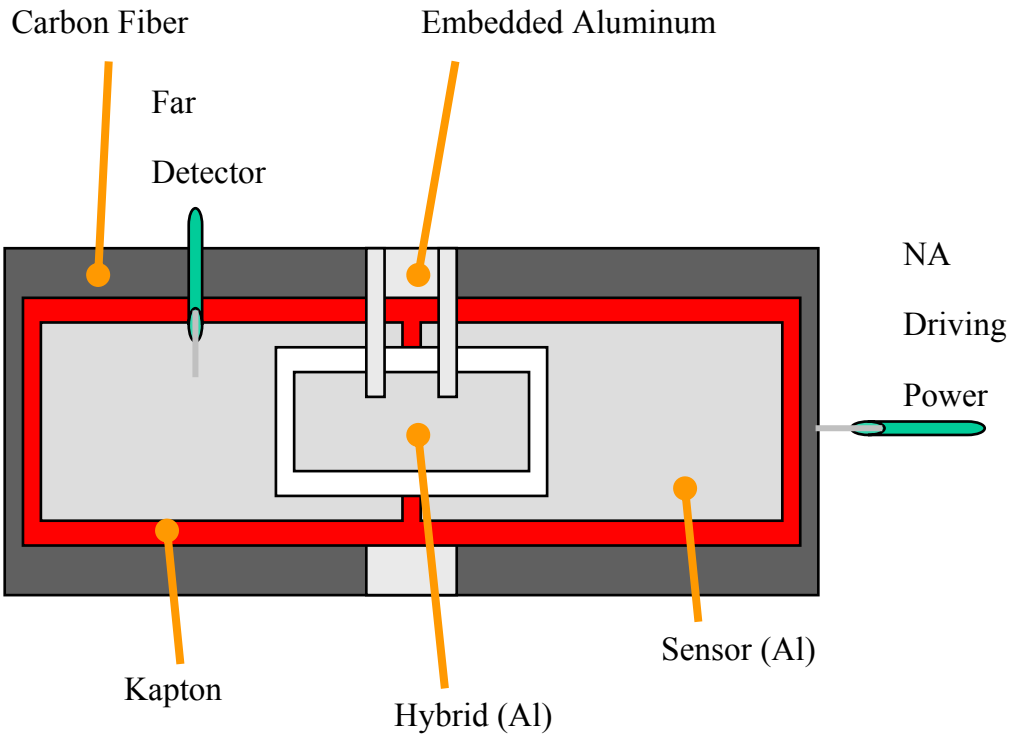


Figure 134. Embedded aluminum coupling contact test setup.

Aluminized Mylar grounding produced significantly less attenuation than aluminum; about 10 dB less below 20 MHz. This test also verified that the attenuation is not affected by the size of the grounding strips. Measurements of transfer functions were taken with different areas of embedded aluminum and equal sized grounding strips. Those data confirmed that the attenuation increases with contact area to the carbon fiber. The maximum area of embedded aluminum tested was 4 in^2, giving a power decrease of at least 30 dB for all frequencies below 50 MHz. Coupling to carbon fiber through embedded aluminum has thus been shown to be an effective grounding technique, although the optimum area of embedded aluminum is yet to be determined.

6 PRODUCTION AND TESTING

6.1 Overview

This section describes the full chain of testing of the individual components needed to build silicon readout modules and the assembly of the components into modules and staves. The building and testing sequence is described, starting from individual components, resulting in fully certified staves. It relies on the successful production and testing effort DØ organized during the construction of the Run IIa Silicon Microstrip Tracker.

The essential building blocks of a detector module are the silicon sensors, the SVX4 readout chips, and the readout hybrids. Each component is tested as described below before it is assembled into a module. After the assembly the modules are tested again before they are mounted on staves. A detailed description of the stave assembly and installation is included in Section 4.4. Testing of staves and of the full readout system are also included below.

The basic production and testing sequence is the following:

1. SVX4 chips are tested as described in Section 5
2. Bare hybrids are tested for continuity and shorts by the manufacturer
3. 100% (5-10%) of bare preproduction (production) hybrids are re-tested
4. SVX4 chips and passive components are surface mounted on the hybrids
5. Fully assembled hybrids undergo an initial functionality test
6. Hybrids that pass the functionality test are burned-in at Fermilab
7. Sensors are produced and tested at the manufacturer
8. 100% (5-10%) of the preproduction (production) sensors are re-tested
9. Sensors and burned-in hybrids are assembled into a detector module.
10. Detector modules undergo initial functionality test at Fermilab
11. Detector modules that pass the functionality test are burned-in at Fermilab
12. 5-10% of burned-in detector modules are subject to more detailed QA tests
13. Burned-in modules are assembled into staves (L2-L5) or mounted on support structure (L0-L1)
14. Up to 6 detector modules are read out simultaneously

Each of the steps in the testing procedure is described in detail below.

6.2 Sensor tests

To ensure high quality of the silicon sensors, DØ plans a series of quality assurance (QA) tests to be performed by the supplier and by DØ. The complete description of the silicon sensor QA program, including detailed instructions, procedures, implementation rules and responsibilities can be found in[30]. A summary of these activities is included in this section.

Quality assurance will be a collaborative effort and is shared among different institutions. The institutions participating in the QA program provide for silicon sensor testing centers, where the quality checks of the QA program will be carried out in a consistent manner. Fermilab serves as a central distribution and control center with dedicated testing and coordinating tasks. Fermilab and two additional remote sites are available as backup locations to perform the standard QA testing of sensors if needed. Figure 135 shows a graphical representation of the QA program with the silicon sensor flow during production.

[30] See http://d0server1.fnal.gov/projects/run2b/Silicon/www/smt2b/Testing/testing.html under Sensor Quality Assurance Procedure

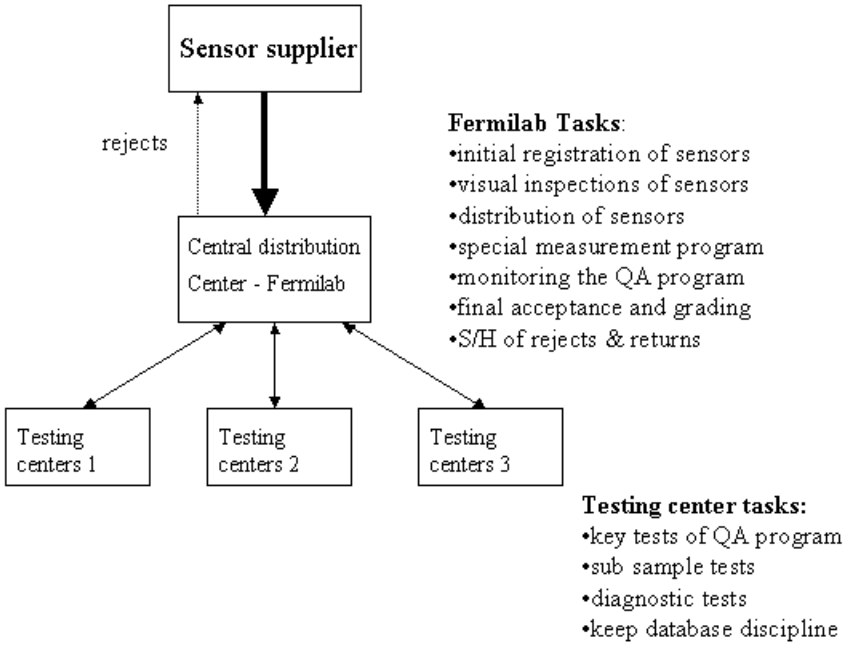


Figure 135 Graphical representation of the sensor QA testing flow

The following paragraphs describe the tests that will be performed by the manufacturer, the remote silicon sensors testing centers and at Fermilab. All electrical tests will be carried out in a temperature and humidity controlled environment, with the sensors placed in a light tight dark box. The equipment necessary to perform these measurements is summarized in Table 25.

Table 25- Sensor Probing equipment

Dark Box	Mechanical Shop
Keithley 237	Keithley Instruments
Rack Mounting kit	Keithley Instruments
HP LCR 4284A	Agilent
Cable option	Agilent
Test Leads	Agilent
Isolation Vibration Table	Kinetic Systems 1201-05-11
Probe Station	Alessi Rel – 6100, Cascade microtech
Guard Box	self made
Storage	

The following tasks will take place at Fermilab:

- Initial registration of sensors
- Visual inspection
- Distribution of sensors to remote testing centers
- Sensor characterizations on sub-samples, as described in this document
- Shipping and handling of the rejects which are returned to the supplier
- Overall monitoring of the QA program
- Final acceptance and grading of sensors

We expect the manufacturer to perform the following tests:

1) Tests on each sensor

   a) Leakage current as a function of reverse bias up to 800 V at room temperature (T = 21 ± 1°C) and relative humidity (RH) < 50%

   b) Optical inspection for defects, opens, shorts and mask alignment (better than 2.5 μm)

c) Depletion voltage measurement either by measurement of the capacitance between back-plane and the bias ring at 1 kHz frequency as a function of reverse bias, or by similar measurement performed on a test diode produced on the corresponding wafer.

2) Tests on each strip

a) Capacitance value measurement and pinhole determination

b) Leakage current at Full Depletion Voltage (FDV) and Room Temperature (RT)

c) The total number of not working channels must not exceed 1%. Non-working channels are defined as:

i) Pinholes – current through capacitor >10 nA at 80 V and RT

ii) Short – coupling capacitor >1.2 times the typical value

iii) Open – coupling capacitor <0.8 times the typical value

iv) Leakage current above 10 nA/strip at FDV and RT

v) Strips with bias and interstrip resistance values out of our specifications

3) Tests on test structure

a) Poly-resistor value

b) Sheet and implant resistivity

c) Coupling capacitor breakdown voltage

The corresponding quality control data of the tests performed by the supplier will be provided together with each sensor on paper or in a computer readable format agreed upon by both parties. The silicon distribution and control center will initially qualify the sensors according to the test results of the supplier. So-called key sensor tests of the QA program will be carried out independently on every delivered sensor for verification at the testing centers. Additional QA measurements will be performed on a sub-sample of the delivered sensors as described below. Based upon the results of these measurements, the silicon distribution and control center has the ability to reject a sensor within 6 months after delivery. The manufacturer will be notified and upon request the sensors will be returned for re-measurements. Both parties – the supplier and the silicon control center together with the Run IIb silicon sensor coordinators - can agree upon the acceptance of individual sensors if specifications are missed only marginally.

The QA program for silicon sensors will be performed at Fermilab and remote sensor testing centers. It consists of four main parts:

1) **key tests** are performed on every received sensor. The measurements/procedures belonging to this QA part are the most important ones to effectively determine the basic sensor parameters. They include

a) Initial registration of the sensor in the database

b) Visual inspection

c) I-V measurement

d) C-V measurement

2) **subset tests** are conducted on a certain fraction of delivered sensors only. The main goal of the subset tests is to verify the specifications more in detail. The fraction of sensors subject to these tests will be different for prototype or production type sensors, as follows:

   a) During prototype phase the subset sample will consist of a minimum of 80% of all delivered prototypes

   b) During pre- or pilot-production phase the subset sample will consist of 50% of all delivered sensors

   c) During production phase the subset sample will consist of 25% of all delivered sensors. As production progresses, we expect to reduce the rate to10% of all delivered sensors, if the measurements are consistent with those performed by the manufacturer and stable over the time.

   d) The sensor subset tests consist of the following measurements:

      i) Leakage current stability I(t)

      ii) Full Strip Test (AC scan)

      iii) Strip leakage current test (DC-scan)

3) The **diagnostic tests** will be performed on random sensor samples as well as on sensors with observed irregularities in the key or subset sensor tests. The diagnostic tests measure in much more detail complex electrical parameters in order to get a deeper insight into the sensor qualities and to monitor the production process. The diagnostic tests will be routinely performed on 10-15% of the delivered sensors per batch with a minimum of 1-2 sensors/batch. The diagnostic tests consist of the following measurements:

   a) Polysilicon resistor measurements

   b) Strip and interstrip capacitance

   c) Metal series resistance

   d) Implant sheet resistance

   e) Flat band voltage measurements on MOS test structure (if available)

f) Interstrip resistance

g) Coupling capacitor and coupling capacitor breakdown value on test structure

4) The **mechanical test** measurements are introduced to verify the mechanical tolerances on the wafers. They will be routinely performed on 25% of the delivered sensors per batch. Tests will check for

a) Sensor thickness

b) Sensor warp

c) Sensor cut dimensions and cutting accuracy

Only sensors that meet all the qualification criteria will be used to build modules.

6.3 Hybrid assembly and initial tests

There will be 4 different hybrid types used in the Run IIb silicon detector: those for use in Layer 0 (L0), those mounted on the silicon sensors in Layer 1 (L1), those mounted on the axial silicon sensors for Layers 2-5 (L2A), and those mounted on the stereo sensors for Layers 2-5 (L2S). The hybrids consist of several elements, which are assembled to form the final readout unit. The beryllia ceramic substrate contains a multi-layer printed circuit. Passive components are mounted on the hybrid, as well as the custom SVX4 readout chip. An AVX connector allows a jumper cable to be attached to the hybrid which carries the digital signals to the downstream data acquisition system. Approximately 1200 production hybrids will need to be assembled and tested with a breakdown as given in Table 26.

Table 26 Parameters for hybrids for the silicon detector

Hybrid Type	# chips/hybrid	# hybrids needed	# spares ordered	Total # of hybrids
L0	2	144	46	190
L1	6	72	28	100
L2A	10	336	104	440
L2S	10	336	104	440
TOTAL		888	282	1170

The hybrid is to be constructed of alternating thick film layers of gold and dielectric built up onto a beryllia substrate. There are six conductor layers and five dielectric layers on the top side of

the substrate. The gold on the top layer must be aluminum-wedge bondable. Layers of dielectric may be added to the back side of the substrate in order to keep the finished hybrid flat to within 0.05mm. This layer will also aid in controlling epoxy run-out when the hybrid is bonded to the silicon sensors. Total thickness of the finished hybrid must not exceed 1.0mm. Thickness of the metal trace layers is specified to be 7 to 9 μm; ground and power plane layer thickness is to be 4 to 6 μm. The thickness of the dielectric layer is in the range of 40 to 60 μm, with a specified dielectric strength of 650V/mil or better. Laser cutting of the final outline should be accurate to +/- 2 mils; the two notches will have a 10 mil radius at their corners (see Figure 136).

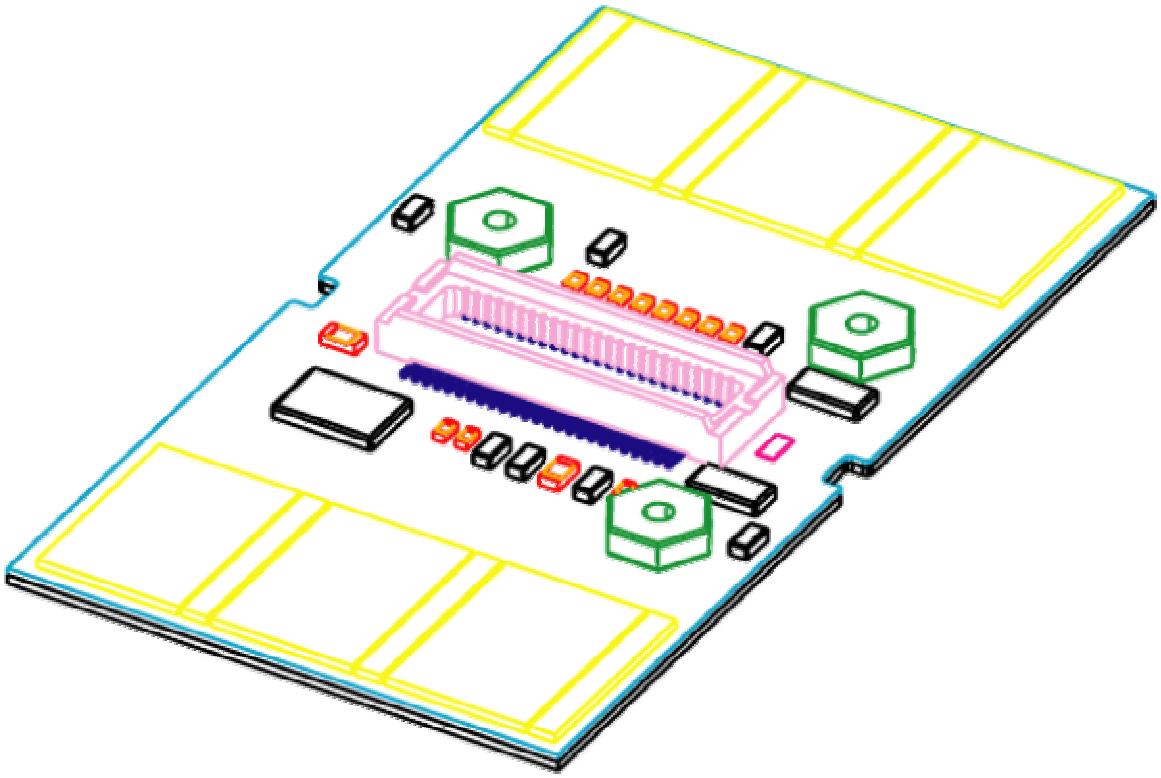


Figure 136: 6-Chip Hybrid

We anticipate using at least 2 vendors for the production of the hybrids. The vendor will test for continuity and shorts before shipping them to the university collaborators for further testing and cataloging. Each substrate will receive a unique identification number and its characteristics entered into a database. The testing starts with a visual inspection. Hybrids will be examined for visual defects and their mechanical tolerances will be checked. A full dimensional inspection will be performed on all prototype hybrids and on a small sample of production hybrids from each vendor run to verify that the substrates meet the required tolerances. The flatness of every bare hybrid will be checked with a go/no-go fixture as this is critical to the thermal performance of the completed modules.

Test stands to check the electrical properties of the bare hybrids will exist at two university locations as well as Fermilab. These test stands will be used to check for continuity and shorts between each of the pads on the substrate and each connector pad. This test stand uses a Rucker & Kolls semi-automated wafer probe station, controlled through GPIB interface with a PC

running LabView. Given a coordinate map of the hybrid circuit, the probe station stage positions each pad under a probe tip, connection is made through a GPIB multiplexing box, and a GPIB controlled multimeter checks for continuity or shorts between the appropriate connector point and the probe.

This testing procedure was tuned for use for the hybrids in the Run IIa SMT detector. The yield of good, bare flexible hybrids used in Run IIa, varied significantly between vendors and between various production batches and ranged from 30% to 100%. For Run IIa it was therefore necessary to test every single bare hybrid. We will have the capability to probe every single ceramic hybrid for Run IIb, but expect that we will only need to spot check around 5-10% of the hybrids before they are sent for stuffing and wirebonding.

6.4 Test stand hardware

Essentially the same type of test stands will be used for all the electrical tests performed on the readout hybrids and the detector modules. These test stands are based on the Stand Alone Sequencer Board (SASeq), which was developed at Fermilab. These SASeq based test stands were successfully used in Run IIa. They are developed independently from the full DØ readout system, and are relatively cheap which allows us to replicate them in large quantities and distribute them at various locations at Fermilab and at remote institutions. The two-channel SASeq board is a self-contained data acquisition card designed to interface to the SVX chips. Its basic function is to control the SVX chip for data acquisition, collect the SVX data when a data cycle is requested, and to relay the data to the processor in the crate. To achieve the planned rate of testing we plan to set up 4 different types of SASeq based test stations:

1. Two hybrid burn-in stations (16 channels each) for burn-in of hybrids

2. Two module burn-in stations (32 channels each) for burn-in of detector modules

3. Eleven 2-Saseq stations (one channel each) for fast functionality test, debugging of modules and QA tests, with 6 stations at Fermilab and 5 at remote institutions;

4. Two 3-Saseq stations (6 channels each) for simultaneous read out of up to 6 modules during assembly of staves and stave mounting in the final support structure

Each Module burn-in station consists of two Cooling Racks and a VME Rack between them. Each Hybrid burn-in station consists of a Shelve Rack and a VME Rack. We plan to reutilize the two racks that were used in Run IIa as Shelve Racks with small changes concerning the electrical parts.

The base hardware unit for the burn-in stations is shown in Figure 137. The Burn-in Crate configuration for module burn-in is shown in Figure 138. It consists of a VME crate that contains a Bit-3 VME controller card, sixteen SASeqs, a scanning 12-bit 64 channel analog-to-digital converter board (VMIVME-3113A) for temperature measurement, and a master vertical interconnect board for high voltage crate control. High voltage supply sources are located in a separate VME crate.

The HV VME crate for the burn-in stations contains four VME 4877PS Motherboards and a slave vertical interconnect board for high voltage crate control. Every Motherboard carries eight HV pods. Thus, the HV crate provides 32 independent voltages for silicon detector biasing and supports monitoring of the detector currents. The 4877PS Motherboard allows the voltage to be set from 0 to 5000 V, with a maximum current of 2mA per channel. To ensure the safe operation of the burn-in stations, the over-voltage hardware protection of the HV supply will be set to 300V.

The interface between the hybrids and the SASeq is provided in Run IIb by a circuit board dubbed the Purple Card. It is the functional analogue of the Interface Card and Connector Adapter Module used in Run IIa. The Purple Card is located close to the device under test inside the Cooling Rack. Every Purple Card has two independent channels and is used as a bi-directional interconnect between the SASeq and the Hybrid through the Digital Jumper Cable (DJC). The board contains the logic to control the power of the SVX chip as well as the HV. The board also prepares the data for the temperature measurement. All low voltages are fused on the Purple Card. The Card is equipped with test points and LED's to monitor the functionality and provide diagnostic capabilities if they require servicing.

Each SASeq is connected to a Purple Card by a 10 foot long 50-conductor cable with impedance of 82 Ohms. Three low voltage power supplies are used to supply the two operating voltages (AVDD, DVDD) needed by the SVX chips and to supply the voltage to power the Purple Card. Low Voltage Distribution wire Buses are located on the side of each Cooling Rack or Shelve Rack and are used for the distribution of the SVX power and the Purple Card power for each of the sixteen Cards.

The Hybrid burn-in station and the Module burn-in station only differ in two aspects, which are the High Voltage crate and the cooling system. The Module burn-in stations need a separate VME crate to house the high voltage modules to bias the detectors, which is not needed for the Hybrid burn-in stations. For the one-SASeq and three-SASeq test stations the HV module is located in the same VME crate as the SASeq. The second aspect in which they differ is the cooling. The Module burn-in stations are outfitted with a cooling system to operate the detectors at low temperature. Up to 16 detectors are placed on 8 shelves inside a Cooling Rack that is thermally isolated. The chiller temperature is set to 5C, and the detectors will run at temperatures between 10C and 15C, depending on the number of chips on the HDI and on the water flow rate. Each detector module is placed on a custom made, 17 x 3.5 inch aluminum Cooling Plate Figure 139, designed to accept any kind of Module. Every Cooling Plate is equipped with a pipe for cooling water and special holes to provide nitrogen flow through the storage box that encloses the device under test. Two Cooling Plates together with the Purple Card and signal cables are placed on plywood board. This board, called the Slider Plate, is equipped with sliders to simplify loading and unloading of the devices under test (Figure 140). Plywood is chosen because it is a cheap, thermally non-conductive material that helps minimize possible risk of condensation on surfaces inside the Cooling Rack. Every Slider Plate has its own water and nitrogen pipe.

A control panel attached to the rack side provides control of the water and gas flow. One chiller supplies two control panels. A software based interlock system monitors the temperature on each device and shuts off the power in the event the temperature exceeds 50C, to avoid melting of the epoxy used in detector assembly.

We have ordered 60 additional Saseq boards; these will be tested at remote institutions following the procedures outlined in Ref. [31]. Additional HV parts are being ordered for use in the test stands. They will be used in the detector when production is finished. The Purple card is currently being designed. A floor plan of the burn-in stations in the Sidet Lab AB-bridge is shown in Figure 141.

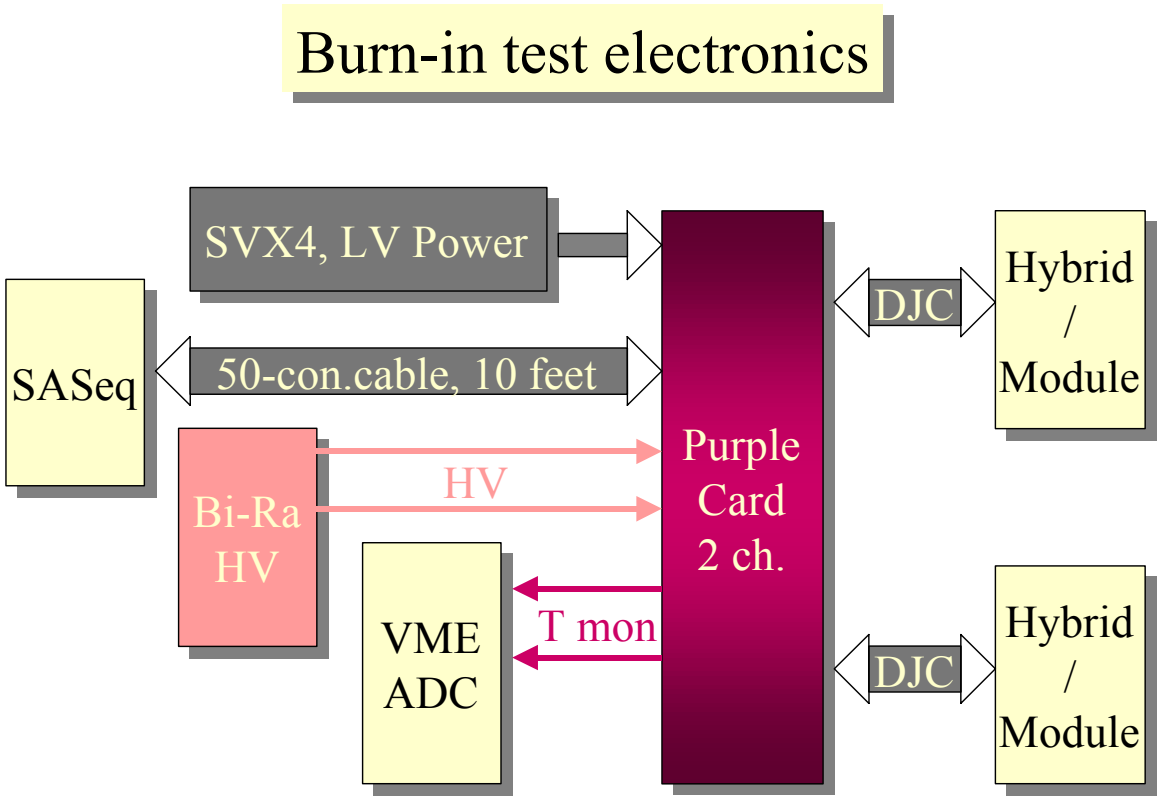


Figure 137 - Base Unit of Burn-In Test Electronics

[31] See http://d0server1.fnal.gov/projects/run2b/Silicon/www/smt2b/Testing/testing.html under Saseq Test Procedure

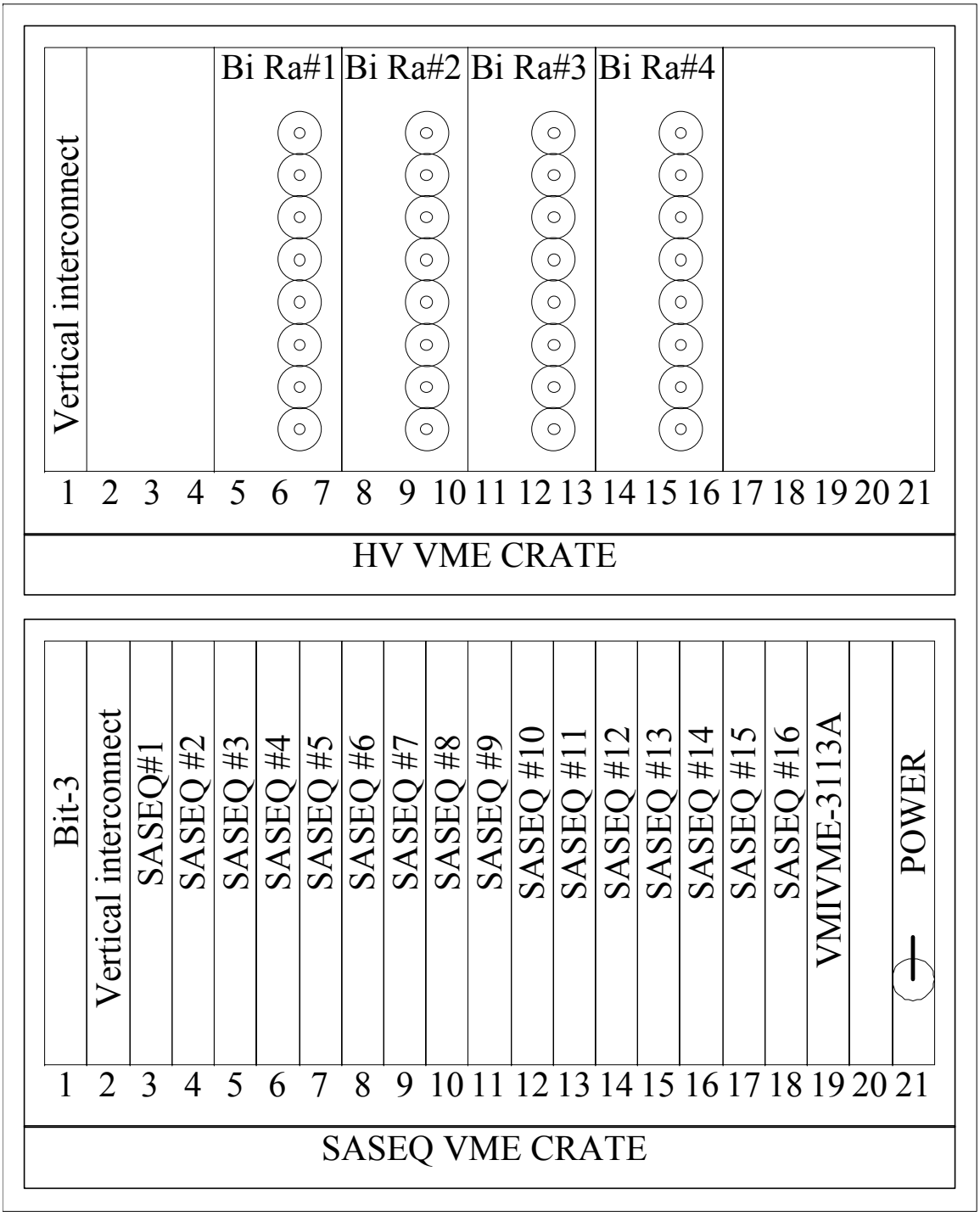
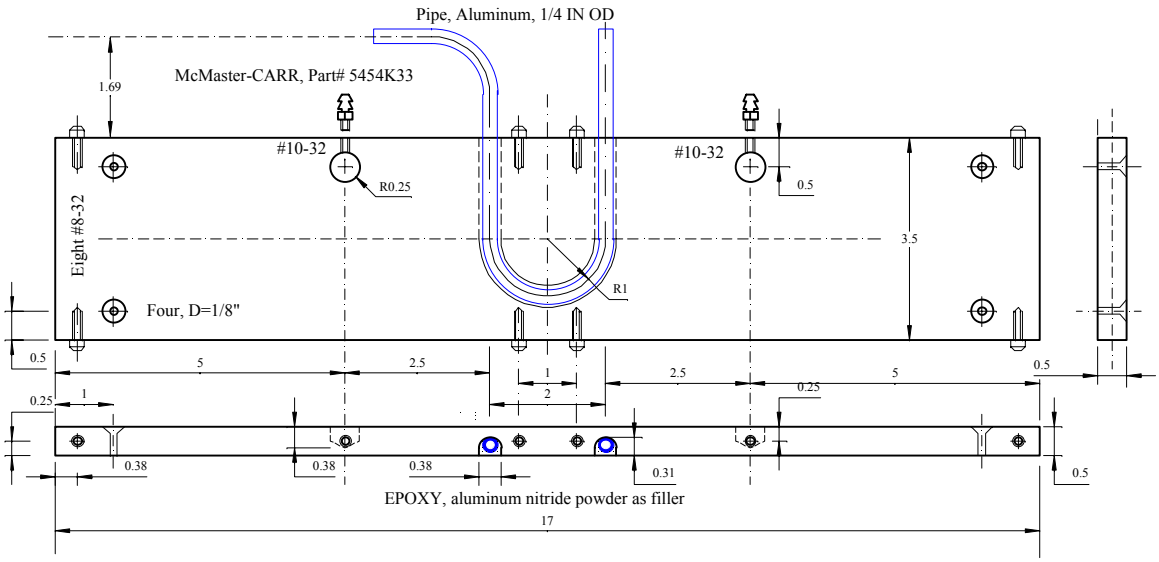


Figure 138 - Burn-in Test Crates.



BURN-IN TEST Cooling Plate.
ALUMINUM, 17 x 3.5 x 0.5 INCH

Figure 139 - Cooling Plate

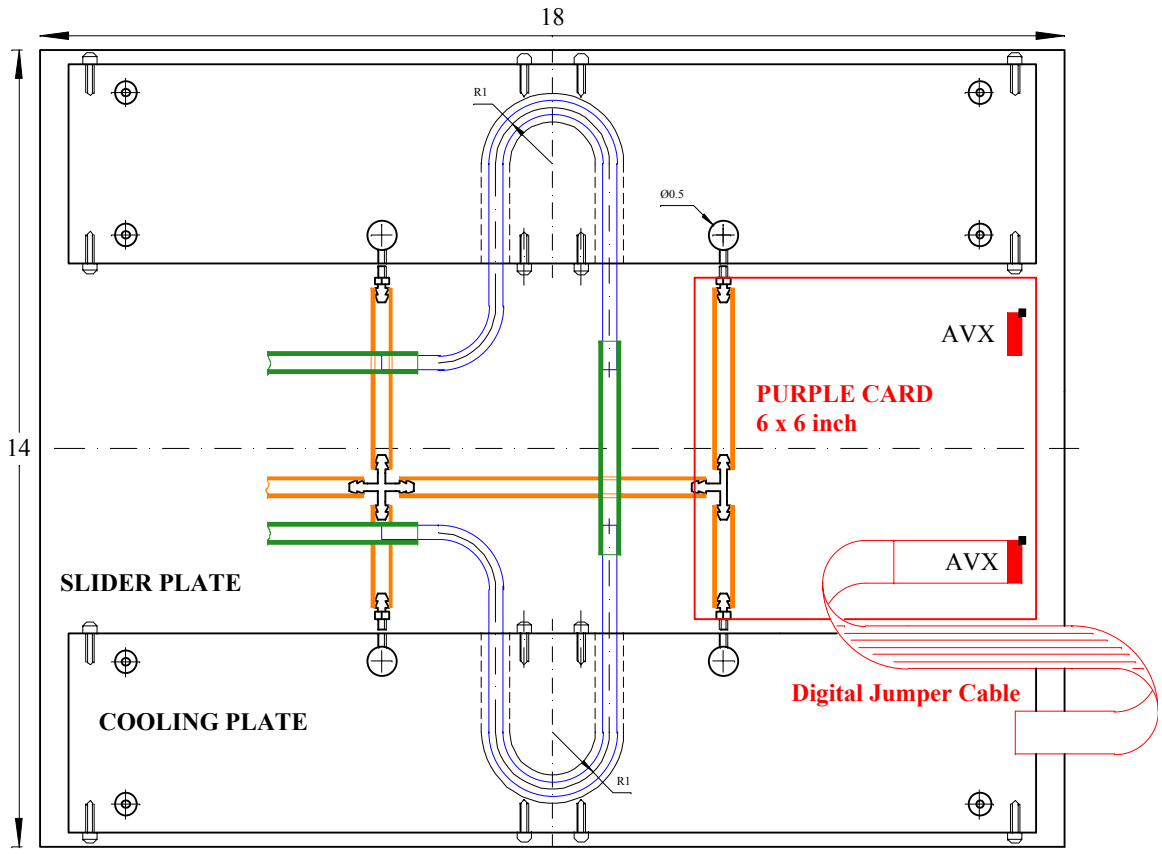


Figure 140 - Slider Plate

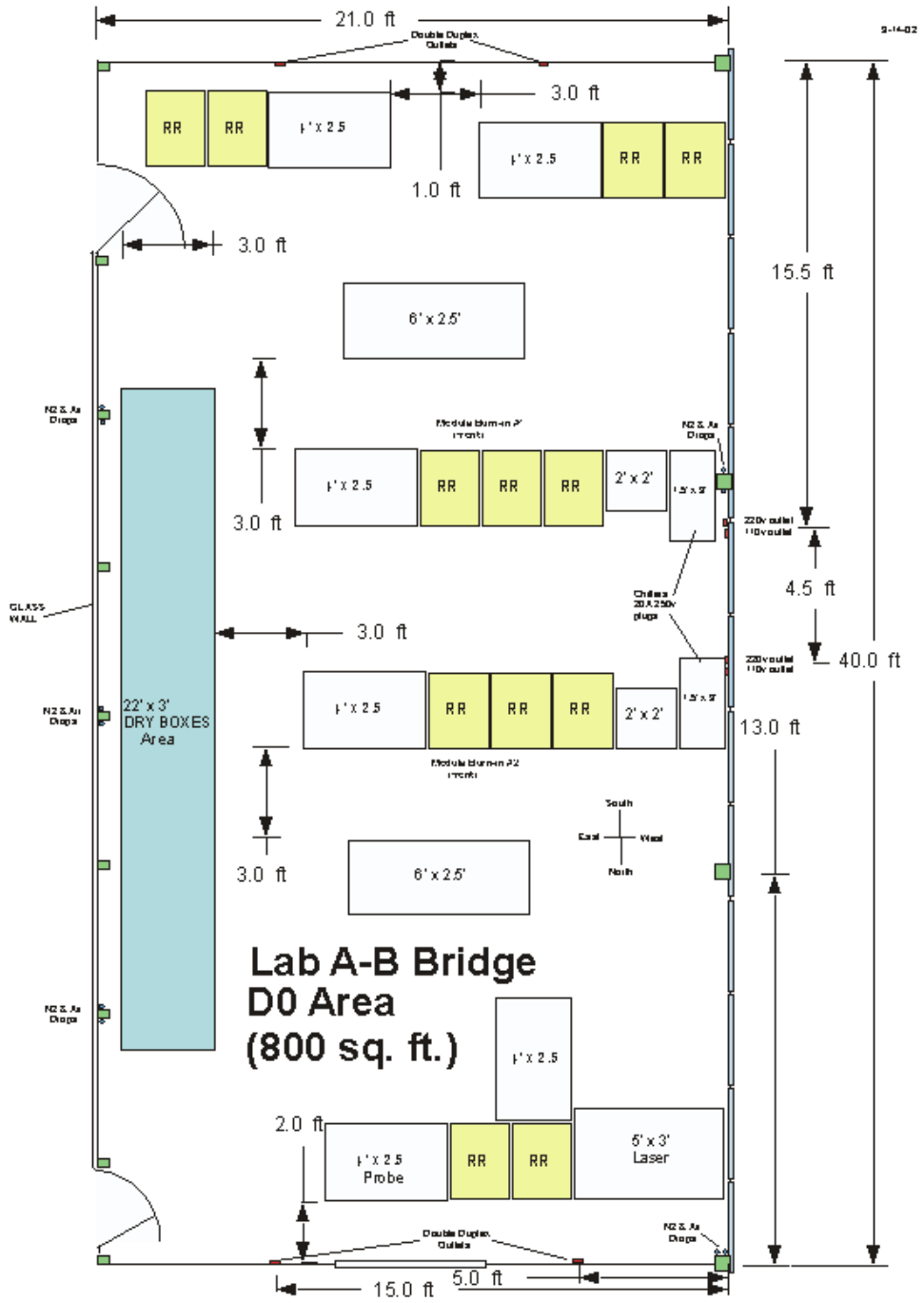


Figure 141 - Layout of Burn-In stations and QA stations in the new SiDet LAB AB Bridge

6.5 Fast functionality test for stuffed hybrids

Once the bare hybrid is ready for surface mount of components, it will be shipped to the stuffing vendor. The vendor will surface mount the passive components, including the AVX connector, using a pick and place machine, perform a simple continuity and short test, attach the SVX4 die to the beryllia substrate using silver epoxy, and then wirebond the SVX4 chip to the substrate. The vendor will ship the finished hybrids back to university collaborators for functional testing.

The initial functionality test at the collaborating universities includes a visual inspection (to ensure that the components were mounted correctly and wire bonds were made to the right pads), and examination of distributions of pedestal and noise as a function of channel number for each of the SVX4 chips on the hybrid. The behavior of the hybrid will also be tested using a large number of successive downloads and in cal-inject mode. Students and technicians at two universities are currently in training to conduct these tests.

The visual inspection is done using a high powered microscope. The purpose is to obtain quick feedback for the stuffing vendors, including general wirebonding problems (too-long tails for example) and to attempt to ameliorate any problems before electrical tests. Typical “repairs" at this point may include manually straightening out bent bonds, identify missing or broken wire bonds for repair in-house, locating SVX4 chips with obvious defects, and also to blow off or pick off debris from previous handling. A K&S manual wire bonder is available at each university hybrid testing site for these quick repairs.

After the visual inspection, there will be a static electrical test to check for power shorts and to verify the connection of the platinum temperature measuring resistor. Hybrids with shorts will be set aside for possible debugging. The functional electronic readout tests are performed using 1-SASeq stands at each university. These stands are already in place from the Run IIa detector and just need to be modified for use with the SVX4 chip. This is the basic test of download and readout. We require 100 successful downloads, and error free readout of 10,000 calibration and pedestal events.

Download failures are, if possible, localized to a single chip using a manual probe station in conjunction with an oscilloscope and logic analyzer, and defective SVX4 chips marked for replacement. Hybrids with problems are scanned at high magnification (50-250X) to search for chip and other defects. For the Run IIa hybrids, in about 50% of the download and readout failures cases, an SVX2 chip flaw was visible. For Run IIa the repair statistics were:

- Diagnostic success was stated to be >70%, meaning that at least 70% of the download and readout failures, when localizable to a single chip, could be recovered.

- About 30% of the hybrids with shorts were recovered, in some cases by burning off debris at “high" current (less than 1A in order not to melt wire bonds), or by manipulation of hybrid tails.

The initial yield of working hybrids that were stuffed for Run IIa was 70% and varied significantly between different hybrid types and batches. The yield after repairs for working stuffed hybrids was around 90%.

The plans for testing are being prepared assuming yields such as those found in Run IIa for the stuffing and wirebonding vendors, which we believe to be conservative. University collaborators will interact with vendors, and perform the initial functionality test and needed repair. Hybrids that pass the functionality test are sent to Fermilab for burn-in. Hybrids that pass the burn-in test are used to assembly detector modules.

6.6 Module Assembly

Information about the depletion voltage and the number of bad strips will be provided as input to the testing and assembly group and taken into account when choosing sensors for a particular detector module. Only those hybrids meeting the desired criteria will be matched to silicon sensors and assembled into detector modules. The techniques for assembly of detector modules will be similar to those used in the past by many groups, including DØ. Sensors will be manually aligned with optical feedback from a camera mounted on a coordinate measurement machine (CMM). Once aligned, the sensors will be glued to one another via a connecting substrate of Kapton or Mylar. The bias connection on the backside of the sensors will be made using aluminized Mylar glued with silver filled epoxy. In the hybrid region this foil will extend beyond the edge of the sensor so that it can be wrapped around the edge and glued to the HV pad on the top of the hybrid to make the HV connection. This is essentially what was done by CDF for the L00 device currently installed in that experiment. The hybrid will be glued directly to the silicon sensors in such a manner that the guard rings are not bridged by adhesive, to avoid any performance problems. Module assembly will utilize 5 Zeiss CMMs for the L1-5 modules, each with a capacity of 2 modules per day. The L0 modules do not require high accuracy alignment as each consist of a single sensor, flex cable and readout hybrid so these can be assembled on a granite surface plate. The total assembly capacity will be 8 modules for L2-5 plus 2 each for L0 and L1 per day, or 60 modules per week, exceeding by more than a factor of two the average production rate we have assumed in our resource loaded schedule. We are investigating high purity, fast curing (<5 hours) adhesives to increase the peak capacity and to more efficiently utilize the equipment and human resources available.

Wire bonding will then be done between the hybrid and the sensors, and from sensor to sensor for the modules with 20 cm readout segments. The sensor pitch is such that the hybrid to sensor bonding can be done directly from the SVX chips to the silicon sensors without a pitch adapter. The total numbers of wire bonds required for layers 2-5 are 353K sensor-to-sensor plus 860K hybrid-to-sensor, for a total of 1213K bonds. We anticipate doing all of the production bonding on a single K&S 8090 machine, with repair work being performed on a K&S 1478. For the longer modules, the sensor-to-sensor wire bonding can be done either before or after the hybrid is mounted. Sensor alignment and sensor-to-sensor wire bonding could therefore proceed prior to hybrid delivery, should that become a production constraint. At several steps during the assembly sequence, the module will be electrically tested, repeating the short functionality test. In order to be able to read out the hybrid, a short digital jumper cable (testing cable) needs to be connected to the module. This will be done after assembly and wire bonding of the detector module, or when an electrical test is required. The connection of this testing cable needs to be done by a skilled technician, as it is a delicate operation that takes place with exposed wire bonds. The testing cable will remain attached to the module during the complete testing process until the module is installed in the tracker and the final jumper cable is connected.

Malfunctioning modules at any step of the assembly sequence will be sent to the repair team for diagnosis and repair. We will consider the possibility that the individual modules may require cooling during the diagnostic tests to avoid over heating. Once a module has been assembled, wire bonded, and a testing cable has been connected, it will be stored in boxes similar to those used in Run IIa. These boxes allow for electrical testing, providing a path out of the box for the digital readout cable, ports in the base for dry gas purge, cooling of the sensors through the base plate of the box and a light-tight seal to allow biasing of the sensors. The modules will remain in these boxes through testing and burn-in and will only be removed when they are to be installed on the staves. Modules can be electrically tested by connecting the testing cable to the purple card, without opening the storage box.

Completed detector modules will be sent to the debugging team to investigate their performance under HV bias. Pinholes could develop during wire bonding and can be removed by pulling the wire bond between the AC sensor pad and the SVX4 chip preamplifier. Because all our silicon modules use single-sided silicon sensors, we expect the debugging of detector modules to be much less demanding than the one required by double-sided sensors. Once the detector module is operational under high voltage, it will be sent for module burn-in.

6.7 Debugging of Detector Modules

Immediately after a detector module is produced, and before it is burned-in, it needs to undergo a functionality test, that we call “debugging”. The likelihood of damaging the detector modules during construction, in particular during wirebonding, is not negligible. An intermediate step between production and before module burn-in is needed to restore the functionality of the modules before performing any electrical tests. The steps we plan to follow during the debugging process are the following.

- Visual Inspection: A thorough visual inspection of the finished module will ensure that no mistakes were made during wire bonding and no mechanical damage occurred.

- Functionality test: this test is done on the module without applying bias voltage to the sensor to assure the electrical integrity of the hybrid after module production.

- Biasing of the detector: bias voltage is applied in 5V increments, monitoring the leakage current. Capacitors that might be broken during wirebonding will be identified during this step. Strips corresponding to broken capacitors will be disconnected from the readout electronics by pulling the wirebond between the silicon sensor AC bonding pad and the SVX preamplifier.

- Characterize the module by producing V-I and V-noise curves and determining the operation voltage.

We plan to have two 1-Saseq debugging stations in the Lab D clean room to check out modules as soon as they have been completed. With an average production for modules of about 30 modules per week, we would debug 3 modules per day in each station, which provides ample time to work on modules that might have been damaged during production. If necessary, both

debugging stations could be manned in two shifts, doubling the debugging capacity, which would allow us to match the planned maximum possible throughput of 60 modules per week.

6.8 Burn-in Tests for hybrids and detector modules

The burn-in test is part and parcel of the testing procedure for module production. It will be performed first on the stuffed hybrid after it has passed the initial functionality test described above. At this point the hybrids are subjected to long term readout cycles. The goal of the test is to select good hybrids for module assembly. The second burn-in test will be carried out after a module has been produced and it has passed the initial functionality test. The idea of the burn-in test is to run every component for a long period of time (up to 72 hours) under conditions similar to those expected in the experiment and monitor its performance, in particular, measure pedestals, total noise, random noise and gain and examine occupancy in sparse readout mode. Other parameters that will be monitored include temperature, chip current, and detector bias voltage and dark current measurement (in module burn-in only). Typical problems that are revealed by the burn-in tests are SVX chip failures, broken and shorted bonds, grounding problems, noisy strips and coupling capacitor failures.

We plan to set up two hybrid burn-in stations, with a capacity of 16 channels each, and two module burn-in stations, with a capacity of 32 channels each. This gives us a total capacity of 96 channels per burn-in cycle, which we consider adequate to accommodate an anticipated production rate of about 30 modules per week, with a maximum production capacity of 60 modules per week. For comparison, our production rate during Run IIa averaged 20 modules per week, and our burn-in capability was 32 channels. We expect to have two burn-in cycles per week, per station, on average. The large volume of information coming from the burn-in tests and the necessity to run the test for many devices requires the burn-in test software to be user friendly so that non-expert physicists taking shifts can operate the burn-in stations. The Run IIa software was based on a user-friendly Graphical User Interface written in the TCL/TK scripting language with the graphical toolkit in the Windows environment. This choice of software interface created a flexible system for performing a variety of tests using executables written in different programming languages, for data taking, monitoring and data analysis. We plan to reuse the Run IIa burn-in software, modifying it for our new modules, and reducing the amount of human intervention in processing the data and storing the information. Given the increase in our production rate compared to Run IIa, we will do most of the processing of data and storage of summary plots in the database automatically.

The different tests performed during burn-in are the following:

- Temperature sensor test: performed at room temperature, before the SVX chip is powered.

- Data integrity check: tests the stability of downloading the SVX chip and verifies chip identification number (ID) and channel numbers of the SVX data for each chip.

- Long term burn-in test: it consists of a number of runs with an idle interval between them in which the chips remain powered. In each run, the SVX chips are tested in “read all” and “read neighbor” modes. In “read all” mode, chip pedestals are read out to evaluate

the noise in each SVX channel and the chip calibration is performed. In sparse readout mode (“read neighbor"), where only the channels whose response exceeds the preset threshold and their immediate neighbors have to be read out, the frequency of false readouts is studied.

For detector modules, this test is performed with the module under bias. For a detailed description of the tests performed during burn-in in Run IIa, see DØ Note 3841. We plan to run the same tests during Run IIb. A Hybrid and Module burn-in run lasts typically 60 hours; the duration might be reduced as production progresses if no failures are encountered and a larger throughput is required.

6.9 QA Test for Detector Modules

Mechanically, all modules will be surveyed using the OGP, an optical CMM with pattern recognition that can quickly measure all of the fiducials on the sensors. This was done with the ladders in Run IIa. This measurement will also provide data on the flatness of the freestanding modules. The modules will be constrained to be flat during mounting on the stave core. The stave core with mounted hybrids is substantially stiffer than the individual components so that we expect to have very flat module assemblies in the finished staves. A number of completed staves will be inspected on the OGP to confirm that this is the case.

We plan to subject a small fraction (~10%) of detector modules to a thorough set of QA tests. The final set of tests will be developed once prototype modules are being produced. The current plan is to test modules in the following areas:

- Laser test: This test is meant to verify the response of the silicon sensor to a light signal. Detector modules will be placed on an x-y movable table enclosed in a dark box, biased and illuminated with a highly-collimated pulsed IR laser, providing a detailed test of each strip of the detector module in a functional setting. The same system was used during Run IIa. It is based on a 1-Saseq test stand, with the addition of the movable table, dark box, and Laser. The solid state laser operates at a wavelength of 1064nm, a wavelength chosen because the high resistivity silicon used in the detectors is partially transparent to it. The attenuation as a function of silicon thickness has been measured, resulting in an attenuation length of 206μm. This laser will thus test the whole depth of the 320μm thick detector and not just a surface layer. We plan to do a detailed scan of the modules to check for uneven response of the sensor to the laser.

- Temperature cycles: The cooling provided during burn-in is only meant to avoid mechanical and electrical damage to the modules. The modules will run at a temperature between 10 and 15C, depending on the number of chips. We consider that a detailed temperature cycle test, in which modules are read out and checked for mechanical integrity after being subject to temperatures of –10C, is desired.

- Probe testing: We do have the ability to probe test silicon sensors after they were assembled into modules, or to do detailed checks of signals in the SVX chips by means of a logic analyzer and a probe tip. We can use this tools for QA tests if found appropriate once we gain experience during the R&D and pre-production phase.

- Pull Tests: we will test wire bonds on the hybrids and between hybrids and sensors on their pull strength during the R&D and pre-production phase, and might consider doing it in a small fraction of modules during production if needed.

6.10 QA Test for Stave Assembly

For the detector modules from Layers 2-5, two axial and two stereo modules will be mounted on a stave before the stave is inserted in the bulkhead. The stave assembly sequence is a 3-day process, with an intended average production rate of one stave per day. The stave production capacity is 2 staves per day. On the first day the axial modules are pre-tested and then aligned and glued to the stave core. While the adhesive is wet, a quick functionality test may be done to ensure that no damage was done to the modules during mounting. In Run IIa this was done, but there were few instances of problems not associated with recognized human error. The remaining problems were related to migration of conductive adhesive being used to mount the ladders, which will not be an issue in Run IIb where we will be using non-conductive adhesive. On the second day the axial modules will be tested, the stave will be flipped and pre-tested stereo modules will be mounted to the stave. On the third day the stereo modules will be tested and then the structural elements will be glued to the stave. After this the stave will be tested with simultaneous readout of all 4 modules. The module installation requires high precision optical feedback for alignment. We anticipate doing this work on the new Browne and Sharp CMM that has been ordered, or on the LK machine in Lab C. The other machine will be used for installation of L0 and L1 modules, which mount directly to the castellated cylindrical support structures.

6.11 Electrical Tests during Stave and Tracker Assembly

We plan to do two types of tests on the modules during stave assembly. Both tests will be performed using a 2-Saseq test stand located in Lab C, close to the stave assembly stations. The first test will be performed on individual modules, immediately before and after installation on the stave. The second test will read out the four modules simultaneously after installation on the stave, to check for cross talk and grounding problems. Layer 0 and 1 modules are not installed on staves, but are mounted individually on the support structure. We plan to perform the same two types of tests during assembly (single module and simultaneous readout of in this case 6 modules), using a 3-Saseq test stand located in LabC, close to the L0/L1 assembly station. The steps of the single module test will be specified following the procedure used during insertion of ladders into the Run IIa SMT bulkhead (see Ref. [32]), and are summarized below:

1. Temperature sensor check at room temperature: ensures that the temperature sensor on the module is working properly. This test is done before the chips are powered.

2. Download of SVX chips for data mode operation

[32] See http://d0server1.fnal.gov/projects/run2b/Silicon/www/smt2b/Testing/testing.html under Procedure for ladder Assembly into Barrels for the SMT

3. Check channel and chip ID
4. Take 100 events in data mode. Check for uniformity of pedestals and noise level
5. Download of SVX chips for cal-inject mode operation
6. Take 100 events in cal-inject mode. Check for uniformity of pedestals and noise level
7. Bias the detector to the operation voltage (depletion voltage + 5V)
8. Repeat steps 2 to 6

After four L2-L5 modules are installed in one stave, or 6 L0/L1 modules are installed on one sector of the support structure, they will be connected and read out simultaneously, to check for crosstalk and grounding problems. Cooling of the modules during assembly and testing will be done with water at 3C. Details still need to be understood to minimize the number of times cooling is connected and disconnected during the assembly process.

6.12 Full System Electrical Test

All the tests described so far on stuffed hybrids and detector modules during production and assembly of the tracker are performed using Stand-alone (Saseq) based test stands.

These tests are aimed at testing a large number of detector modules extensively and with redundancy in order to detect problems and fix them. The production testing needs to be complemented with a test of the real readout chain, the one that will eventually be used for the data acquisition in the experiment. This test is described below.

We plan to test the full readout chain with a maximum achievable number of full staves , or an equivalent number of stuffed hybrids, through all of the components of the final readout chain. The goal of this test is to understand the full readout system and perform modifications well before the system needs to be operated in the collider. The same idea was behind the so-called 10% Test during the production of the Run IIa detector, which was crucial in understanding the data acquisition system. At that time, a large number of components that were eventually installed in the detector were used for the test. Because we are reusing a fair amount of components for Run IIb, we cannot plan on a large-scale full system test like the one we had during Run IIa. The added cost of the equipment to test 10% of all readout channels would be prohibitive. Nevertheless, we believe that careful tests of the full readout chain are imperative. The SVX4 chip, hybrids, the cabling plant connecting the hybrids to the adapter cards and the adapter cards themselves are all new components requiring testing.

We plan to perform those tests with DØ readout electronics in the Silicon Detector Facility. We will maintain two test stands, which we call the Vertical Slice - Single Unit Full Chain (1%) Test Stand and the Multi Unit Full Chain (10%) Test Stand. The 1% test stand is a minimal setup without the need of a full high voltage or low voltage system. This test stand will include one module of each necessary component to make a full chain test. It is capable of testing up to 2 staves (8 hybrids) or one L0 sector (6 hybrids), or two L1 sectors (2x3 hybrids). The Multi Unit

Full Chain (10%) test stand will increase the number of hybrids tested from 8 to possibly 80. The setup includes all three types of crates participating in the SMT readout: an Interface Board crate, Sequencer crate and VRB crate. The High Voltage System and LV system will be integrated into the test stand as it becomes available. The crates are populated with spare Run IIa boards. The DØ Trigger Framework functionality is replaced with a FPGA board that emulates those functions required. This allows us the flexibility of operating without the DØ trigger framework. Data will flow from the detectors to the SBC and then by Ethernet to a local LINUX based computer. The electronics can be controlled either by software based on Excel spreadsheets or by the Run IIa SMT online software. The Excel based software is currently used by the DØ engineers to debug the hardware while the online software provides a realistic test at full readout speed.

As we start receiving prototypes we plan to perform the following tests using this setup:

- Hybrid with SVX4 chips connected with Jumper Cable to the Purple test card and to the Sequencer. This test is complementary to similar tests with SASeqs. In addition it will allow developing of all firmware changes for production Sequencers before we receive other prototypes.

- Full readout chain: Hybrid – Jumper Cable – Junction Card – Twisted Pair Cable – Adapter Card – 80-conductor cable – Interface Board – 50-conductor cable – Sequencer. These tests are crucial to verify the performance of all components. The timing studies are especially important to verify the impedance matching between different components and the signal terminations.

- Multi-channel readout test. We have capabilities to install several Interface Boards, Sequencers and VRBs, up to 10 boards of each type (80 readout channels). The exact number will be limited by the amount of spares that we will be available to use. In order to connect a sizeable number of hybrids and/or detector modules we will need to provide adequate cooling and a light-tight box.

6.13 Production Database

The amount of information that we need to keep track of during the construction of the DØ Run IIb silicon tracker arises mainly from the number of components in the device itself, but also on the rather large number of vendors and universities involved, and the need to maintain a stringent and uniform quality control. We are designing a production and testing database to store all the information relevant to the production and testing.

We have set up a Linux server for this purpose. We have designed a relational database using mySQL, where each item (hybrid, sensor, module, stave, etc.) has its unique ID for easy identification and tracking. We then use PHP to provide a web-based interface to the database. Every object entered into the database will become an entry in the ITEMS table, containing information about type of object, location, status, etc. For each test performed on an item, an entry will be generated in the TESTS table. Test results on various formats will be stored directly in the database. The access to the database will be web-based. Any user will be able to DISPLAY information, but the EDITING of information will be password protected. HISTORY

will be available for every item, and also for all editing done by a particular user. For the design of this database, we're following the description of the ATLAS Silicon Tracker production database[33].

[33] http://www.hep.man.ac.uk/groups/atlas/SCTdatabase/Database.html

7 RADIATION AND TEMPERATURE MONITORING

All silicon detectors will eventually be rendered inoperable or develop inferior performance due to the effects of radiation. Care must be taken to minimize the effects of radiation and to avoid unnecessary and premature damage. The most important parameter to control the effects of radiation damage is the operating temperature of the silicon. Since the front-end readout electronics is, in most cases, mounted on the silicon sensors, the danger of excessive heat and possible thermal run-away is always present. Without adequate cooling the energy dissipation in the front-end electronics could swiftly render the detector useless for physics. Less extreme heating, while not causing catastrophic damage, can greatly exacerbate the effects of radiation damage. For these reasons, the monitoring of currents, temperatures, and radiation dose are crucial to the safe and reliable operation of the detector. In Run IIa, currents, temperatures, voltages, and radiation dose from the accelerator are all monitored. Currents and temperatures are interlocked at several levels, so that deviations from set limits will trip off the appropriate power supplies. The radiation monitor has the ability to abort the Tevatron beam if radiation dose levels reach unacceptable levels. Some modest improvements are planned for the radiation and temperature monitoring systems for Run IIb silicon, consistent with the changes in detector design, as described below. The current and voltage monitors from Run IIa will be retained for the Run IIb detector.

7.1 Radiation Monitoring and Beam Abort System

7.1.1 The Run IIa system

A radiation monitoring and beam abort system is currently in operation for Run IIa. This system consists of two mostly independent subsystems: a system based on the Beam Loss Monitors as they are used by the FNAL beams division, and a system based on silicon diode sensors. Both systems are independent up to a last stage, where the output of both are recorded in the same data stream and where a combination of the information of both systems can be made to trigger a Tevatron beam abort. An overview of the current system is given in Figure 142.

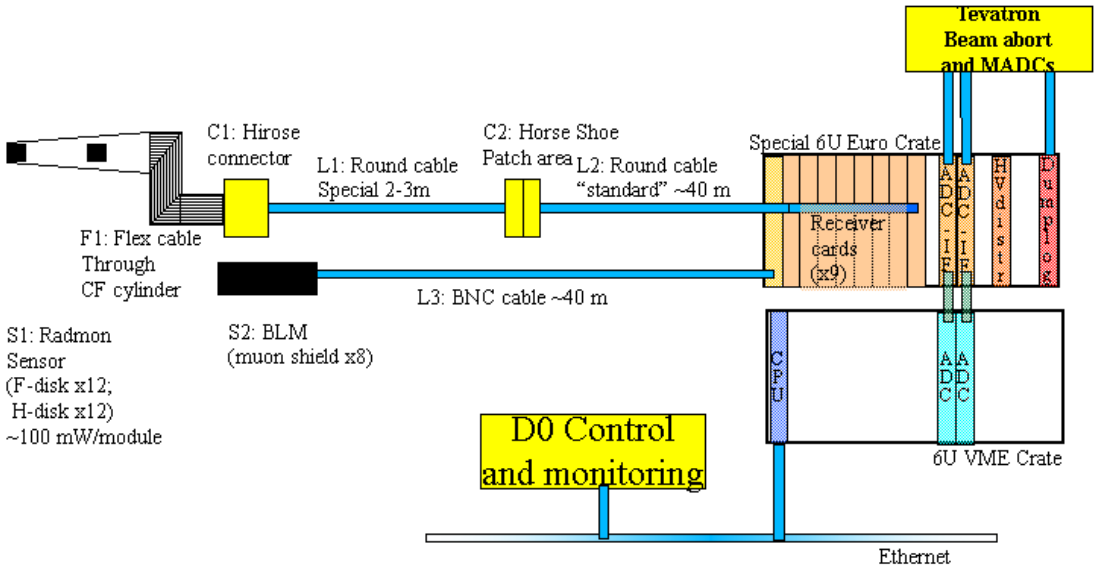


Figure 142 - Overview of the Run IIa silicon radiation monitoring system

The Beam Loss Monitor (BLM) System consists of two sets of four glass cylinders filled with 1 bar Ar gas. On either side (north and south) four BLMs are placed at 3, 6, 9 and 12 o'clock positions around the beam pipe, inside the shielding of the forward muon chambers. Radially they are about 12 cm away as measured from the nominal beam position to the center of the BLM tubes. Their position along the beam direction is about 4 m from the nominal average interaction point. The position of the BLMs is sketched in Figure 143.

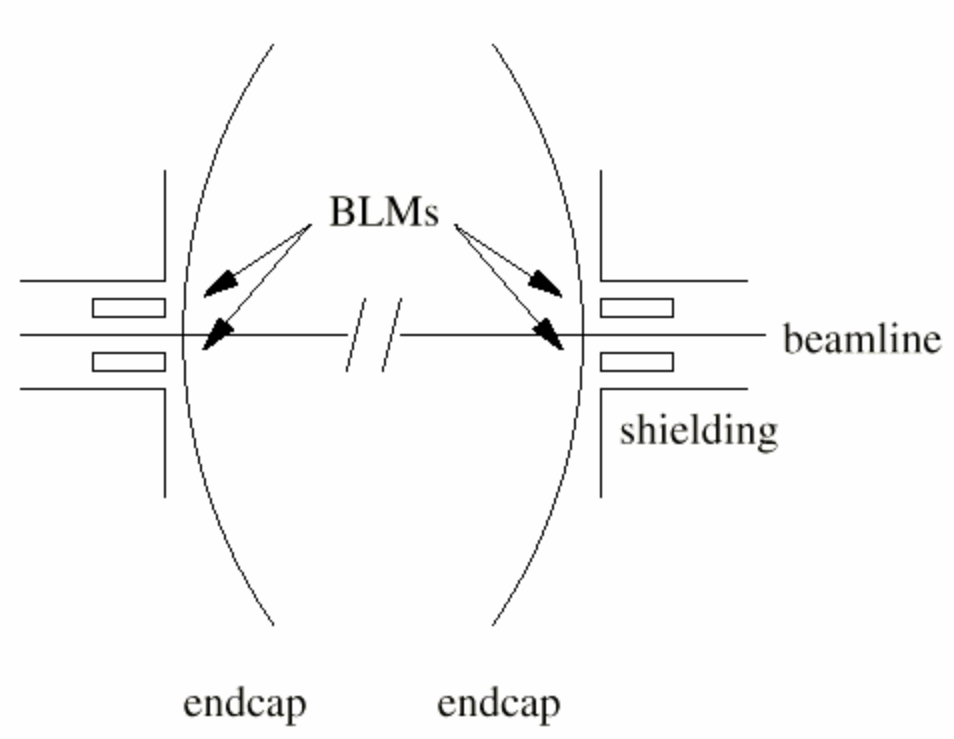


Figure 143-Location of Beam Loss Monitors

In the gas volume two concentric cylindrical nickel electrodes are placed and put under a voltage of about 2 kV. This arrangement causes a current to flow when ionizing particles traverse the gas in the glass cylinder. This current is proportional to the number of ionizing particles through the volume per unit time. The dark current of this arrangement is extremely low, allowing sensitivity down to the single particle level. The high voltage is supplied to the two groups of four BLM tubes with a single high voltage cable and a daisy-chain configuration at the tubes. Because of the low dark current and the limited voltage drop in case of radiation, the high voltage of the tubes is protected, such that the current never exceeds 0.03 mA. For each BLM tube a single BNC cable carries the signal running to electronics located in movable counting house 2, which can be accessed at all times. Currently the output signal is connected to standard beam division electronics C336 modules, which functionally consists of a slow (0.94 s time constant) logarithmic integrating circuit. The processed signal is also fed into a C335 discriminator module that triggers the Tevatron beam abort.

In the near future we expect to connect the BLM outputs to our own electronics. This electronics consists of linear amplifiers with different scales to cover the large dynamic range desired. The advantage of this system compared to the Tevatron electronics is that the outputs will be recorded in the same data stream as that of the other system, the silicon diode sensors. Also the fast time structure of the signals will be used by sampling at a few kHz rate, allowing a more detailed trace-back in case of a beam abort. It will be possible to combine the BLM information and the silicon diode sensor information into one beam abort system, thereby allowing the system to be both more reliable and robust.

Because of their position relatively far away from the interaction point and the SMT, the BLM system does not necessarily give the correct indication of the radiation levels at the SMT. Nevertheless, a large fraction of the times that excess radiation was observed, the time structure of the levels recorded from the BLMs and the silicon diode sensors, mounted directly on the detector itself, were similar.

The Silicon Diode Sensor System are also know as the radiation monitoring fingers (radmon fingers), because of the shape of the sensor boards.

The front-end sensor boards are finger shaped to fit in between the F-disk modules and H-disk modules of the current SMT. On both the north and south side of the experiment, six radmon fingers are mounted on the outer F-disk plane (F-disks 1 and 6) and on the outer H-disk planes (H-disks 1 and 4). A picture of one of the finger is given in Figure 144.

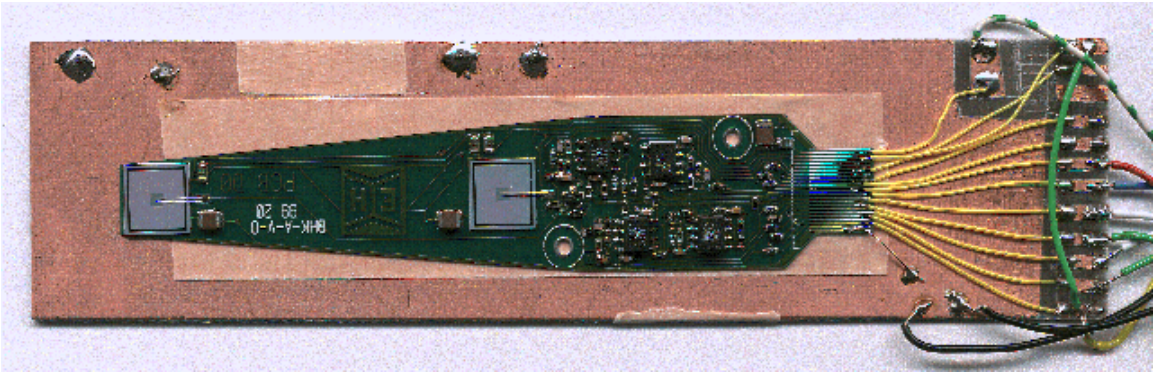


Figure 144-Radiation monitor finger

The fingers each contain two diodes that are read out individually and are placed at a different radius. The radii of the diode positions are arranged such that the inner H-disk diodes are at the same radius from the beam as the outer F-disk diodes. The inner F-disk diodes are at radius 2.6 cm from the beam, the outer F-disk and inner H-disk are 9.5 cm from the beam and the outer H-disk diodes are 16.5 cm from the beam position. In the direction along the beam the F-disk fingers are located at 55 cm from the average interaction point and the H-disk fingers are at 120 cm. The mounting on the F-disks is shown in Figure 145.

Figure 145-Mounting of radiation monitor fingers on F-disks

The silicon diodes have a square active surface area of about 0.7 cm^2. The diodes are fully depleted by reverse biasing them. In that state charge that is freed by ionizing particles passing through the material is collected as electrons on one side of the diode and holes on the other side. The subsequent signal has a rise and decay time of less than 100ns total, and the signal height corresponds to the total charge, which in turn is proportional to the number of ionizing particles crossing the diode. This signal is pre-amplified locally on the diode card with two different gains to increase the dynamic range. The electronics has only one type of amplifier as the active component, and this amplifier was chosen specifically for its radiation hardness (at least several MRads) and its large gain-bandwidth product (about 1 GHz). A schematic layout of the diode board electronics is shown in Figure 146.

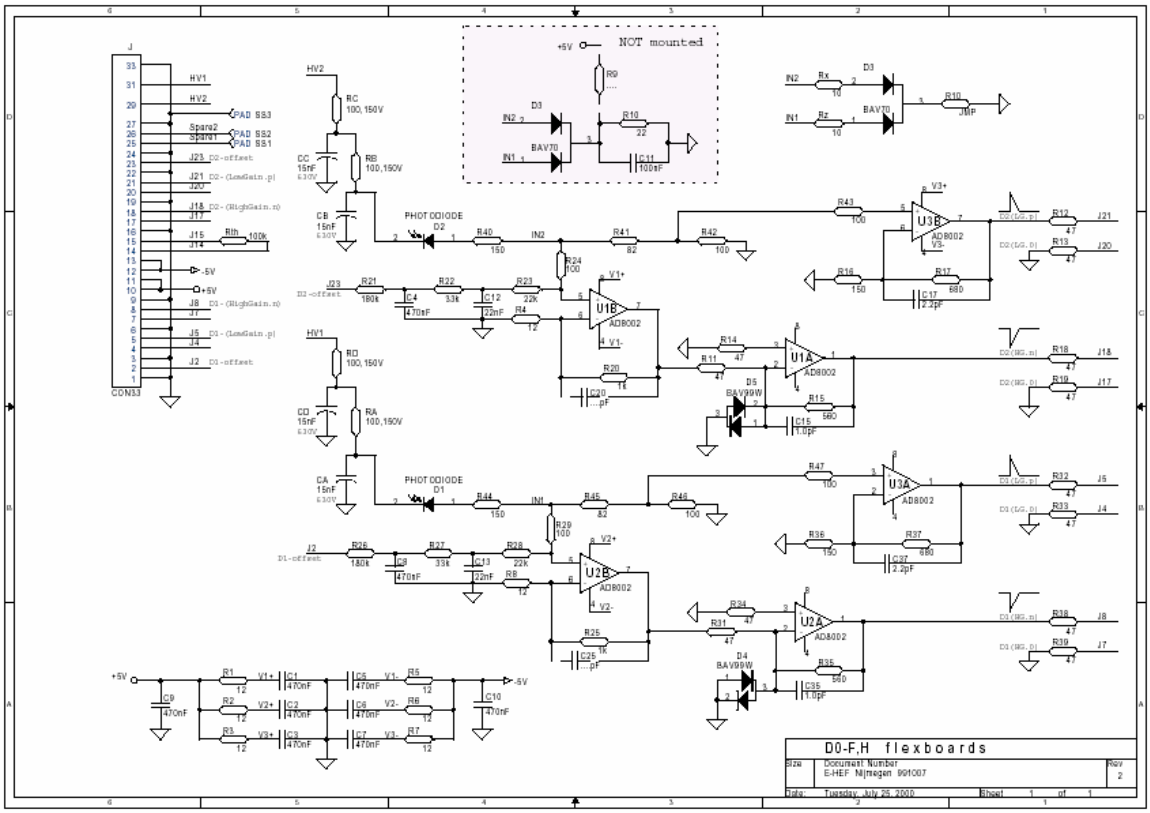


Figure 146-Schematic of diode board amplifier

The diode boards are mounted such that they have very good thermal contact to the cooling ring of the F-disk. The diode boards are constructed from thin printed circuits on polyimide, which is laminated onto thin Be cooling plates of the same size. Because the dissipation of the diode cards is small, they maintain a significantly lower temperature than the F-disk modules of the SMT. Since the silicon diodes are of the same material as the SMT sensors they are expected to have a longer life since they are maintained at a lower temperature.

In addition the electronics is set up such that large leakage currents that may flow into the amplifier can be compensated externally from the counting house. By monitoring the dark current from the amplifiers and adjusting the compensating current, several mA can be taken out of the 0.7 cm^2 diodes, which corresponds to a radiation damage level at which the SMT itself will have died. To keep the diodes depleted, even after radiation damage, the system allows a bias voltage up to 300 V.

The linear signals from the diodes are base line corrected by electronically differentiating and then integrating them again. This makes the system robust against slowly varying (response time more than 100 kHz) currents in the diodes, which may arise, for example, from temperature fluctuations. The signals also pass through a low pass filter with cuts off contributions to the signal with frequencies above about 1 GHz. To be sensitive to even a single minimum ionizing particle passing through the diodes, scalars are connected to the channels, counting pulses above a certain threshold. The threshold is set to have a pedestal rate of a few hundred Hz at most and to accept about half of the minimum ionizing particles. This allows the measurement down to a

rate of a few microRad/s. The saturation level of the low gain amplifier channel is about 25 kRad, hence the dynamic range of the system is about 10 orders of magnitude.

The signals from the diode sensor cards go to the signal receiver cards. The schematics for one channel of the signal receiver card electronics is shown in Figure 147.

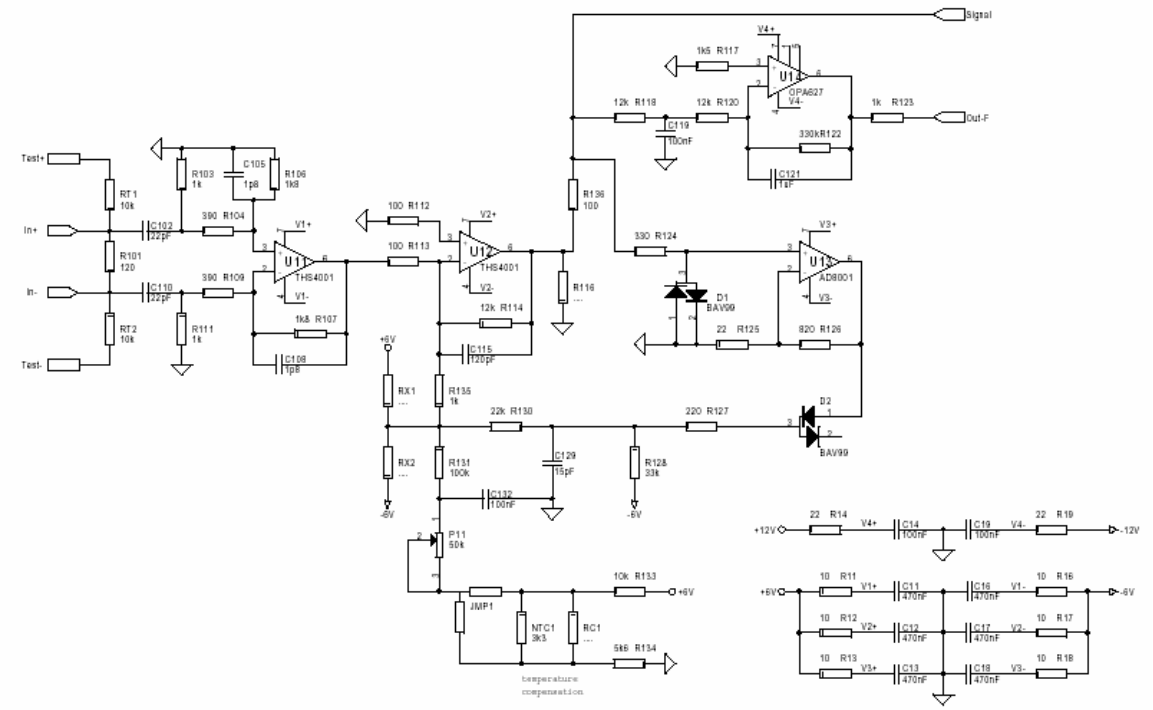


Figure 147-Schematic of the silicon diode signal receiver card

The output signals are split into a set with a fast time response (100 ns) which go to the scalars and the beam abort integrators, and a set that is slower, with two different shaping times, 1 ms and 1 s. The 1 ms shaped signals are sampled at several kHz by an ADC module, and the output is stored in a cyclic buffer. This buffer is read out and stored in case of a beam abort or in other situations that trigger this read-out. The 1s shaped signal is sampled by an ADC at several Hz. This signal is numerically integrated to 5 second averages and injected in the EPICS control and monitoring system, which allows it to be displayed and also stores it into a data base.

The BLM system is calibrated using a strong source to give a signal of 1.1 V at 160 Rads/second. The diode sensors are calibrated by calculating the charge that is released by one minimum ionizing particle in the 300 mm thick silicon diodes, which is about 3.8 fC. The response of the readout electronics is then simulated with Spice using the input signal strength and shape. The calculation is verified by looking on an oscilloscope at signals at the end of the readout chain in response to minimum ionizing particles from a radioactive source. The most probable peak value for minimum ionizing particles, about 30 mV on the fast output signal after the first integration stage, matches within a few percent the predictions from Spice.

In another test, the response of the diode sensor system is tested by injecting signal chains with the same time and amplitude characteristics as measured using minimum ionizing particles from a source. Again the measured response matches the Spice simulation within a few percent.

The final calibration of the system is done in situ using the radioactivity of the Tevatron beams. During normal stable beam running conditions, and during beam off conditions, the number of pulses above a certain threshold for the fast signal is measured as a function of the threshold. This test confirms the most likely signal height of the fast signal of about 30 mV. This is shown in Figure 148, which plots the scalar frequency as a function of the threshold in mV:

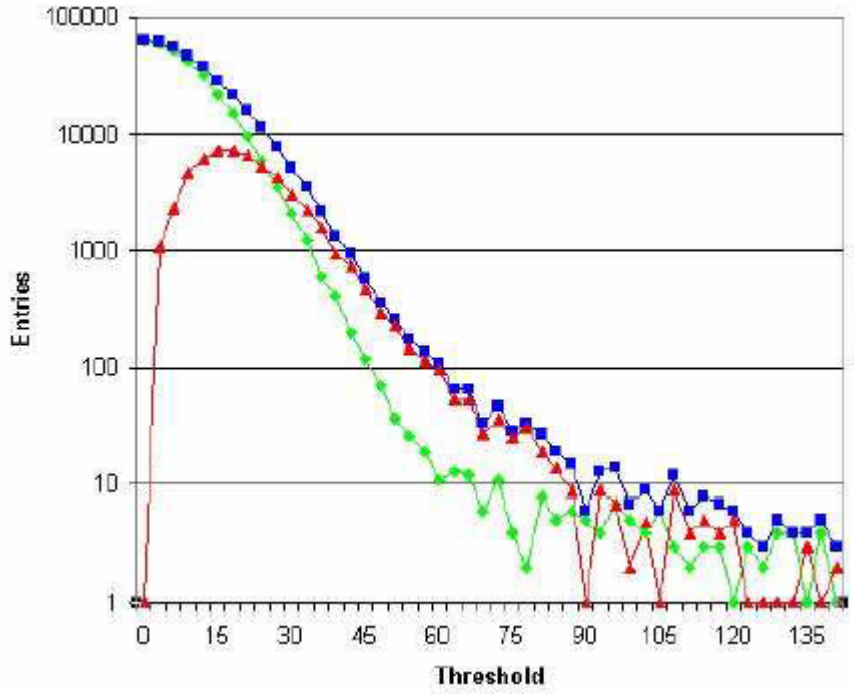


Figure 148- Scalar counts from the silicon diodes vs. threshold in mV for beam on (blue squares), beam off (green diamonds) and the difference (red triangles).

In Figure 148, the upper curve connecting the square (blue) measurement points is the measurement with beam on and hence some background radiation. The curve connecting the diamond (green) points is measured when there is no beam hence no background radiation. The difference between the curves is shown by the red triangles and peaks around 15 mV. This curve was measured using a termination resistor to avoid reflections in the transmission line, but also causing the signal to be halved. Therefore the real peak value is at about 30 mV, in perfect agreement with the prediction from the Spice simulation and test measurements on the bench.

As a qualitative cross check we normally see that the radiation dose rates on the BLMs and the diode sensors track in time. However, the relative normalization varies indicating that the mechanisms of radiation loss are not always the same. Both the BLM system and the diode sensor system appear to be perfectly stable in response from repeating the in situ calibration described above.

An example of signals recorded from the silicon diodes in a mild radiation incident is shown in Figure 149. This figure shows that the dose rate as estimated from the scalar counting rate and the dose rate as measured through the shaping and integration circuit have good qualitative and quantitative correspondence, up to an uncertainty of about 10% in absolute calibration.

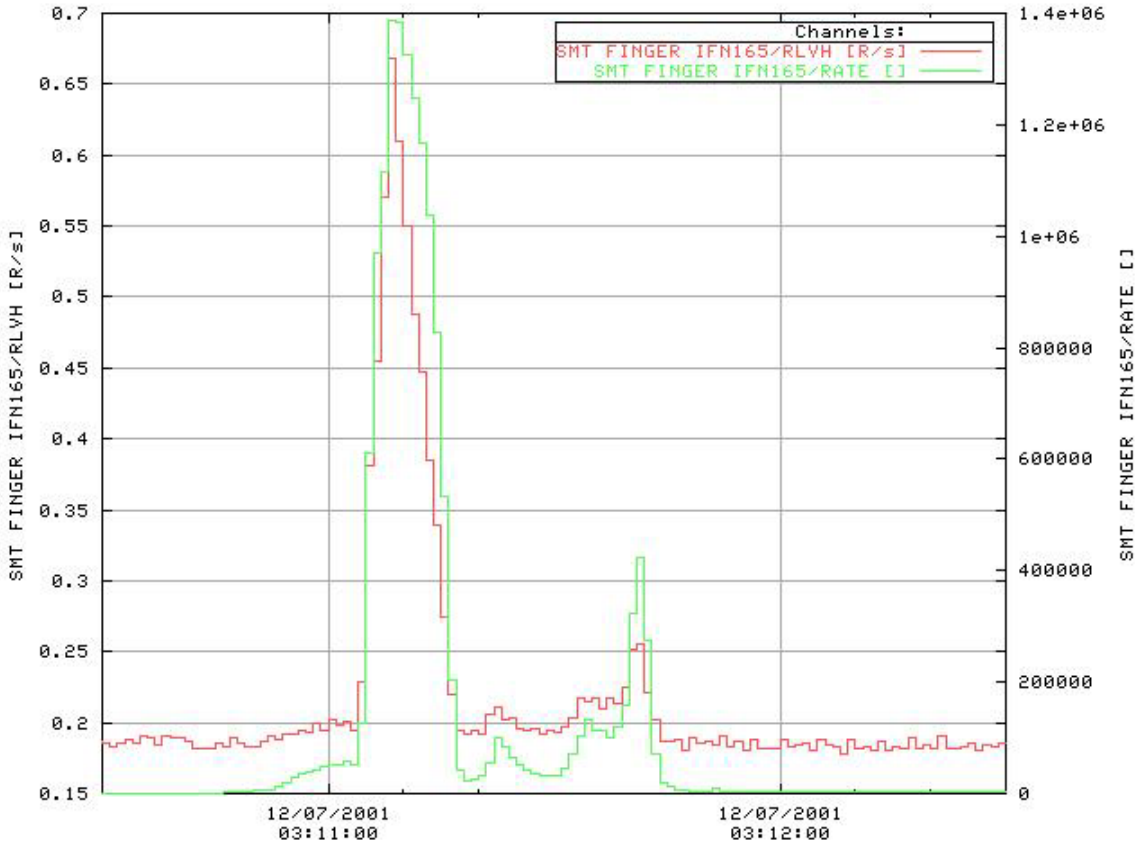


Figure 149- Dose rate from a single radmon finger as measured both by the scalar rate and from the integration and shaping circuit.

7.1.2 The Run IIb radiation monitoring system

In the Run IIb system we will maintain the BLM system as it is. This system is very reliable and radiation hard, so there is no need to replace it.

Also the silicon diode sensor system is expected to perform as well in Run IIb as in Run IIa. Therefore, there is also no need to replace this system, other than the fact that the front-end finger shaped sensor cards are tailored to the F-disks arrangement in the Run IIa detector.

For the Run IIb system these front-end sensor cards will have to be replaced by something that fits the new geometry. The most promising place for the diode sensor cards that has been identified is at the end of the SMT detector barrels. The inner layers of those have less sensitive detector length, yet the geometrical length available is the same for all barrels. This makes it

possible to mount silicon diode sensor cards in the area where the cables attach to the SMT modules.

Replacing the diode sensor cards also makes it necessary to replace the cables between the sensor cards and the interconnection "horseshoe" that is located between the central and forward calorimeter cryostats. These cables have to be made to size, as space constraints are tight.

Redoing the sensor cards allows for some small improvements. In the Run IIa system we can clearly see the detector readout signals as noise in our system. Although the noise level is not jeopardizing the system, we think we can reduce it even further. The main area where the noise couples in at the moment is thought to be the sensor board itself, which is very close to the F-disk modules, but even more likely the low mass HDI cables that are fed through the carbon fiber support cylinder packed together with similar low mass F-disk module cables. These low mass cables consist of polyimide foil with metal circuit traces printed on them. Only one side of these foils consists of a grounding plane, leaving the power, signal and control line traces on the other side electromagnetically unprotected.

In the new system we will cover the diode sensor cards with aluminized polyimide that electrically connects to the ground plane of the signal board, thus forming a Faraday cage. The group shielded cable will be soldered directly to the sensor boards, with the shield connected to the ground plane. These cables, made to the correct size, will connect to the existing connector in the horseshoe.

The design depends only on the choice of the position and shape of the diode sensor cards. A minimum surface area of about 8 cm^2 is needed and the card should nowhere be narrower than 1.2 cm. A cable route has to be found for a round composite cable of 3 mm diameter from each of the sensor cards to a corresponding horseshoe connector. On both south and north side of the detector now more than 12 sensor boards can be accommodated, and we have a preference to use all these slots to have enough redundancy and geometrical information on radiation rates and doses.

Production of the sensor cards and attached cables can start after their position and geometry have been fixed. We intend to produce the sensor cards on thin, but standard PCB material. There is no need for a Be cooling plate as was used for the Run IIa sensors, because the sensors will be outside the active detector area. If needed the PCBs can be laminated onto thin Al cooling plates.

The other critical item for the production of the sensor boards is the silicon diodes. The stock of best quality diodes left from Run IIa is marginal, so all diodes have to be produced. These are diodes of the same material as the SMT detector wafers and are simple multi-guard ring structures. In fact these diodes will be added as test structures on the detector wafers to be procured from Hamamatsu. The diodes will be tested for stability and leakage current behavior, and their depletion voltage will be determined from the CV characteristic.

7.2 Temperature Monitoring

Due to the proximity of much of the electronics to the silicon sensors, temperature monitoring of the detector is crucial. Enough heat is generated by the electronics to easily start a fire if the cooling failed. Moreover, effects of radiation damage can be exacerbated by high temperatures. Remote-sensing devices mounted on or near the sensors themselves are needed not only to continuously monitor temperatures, but also to provide interlocks to shut off power in the event of a loss of cooling or other problem. The temperature-sensing device of choice is a Resistance Temperature Detector (RTD), a thin-film platinum resistor with a high temperature coefficient of resistance. These devices are widely used in industry, stable, reliable, and readily available.

7.2.1 Run IIa Temperature Monitoring

In the Run IIa, the temperature of each High Density Interconnect (HDI) is monitored with an RTD. There are about 900 RTDs in the Run IIa silicon system. They are read out through a two-wire system in which the same leads both supply a DC current and read out the resulting voltage. This readout method, which does not compensate for the resistance of the leads, limits the accuracy to about 1-2C. The analog voltage signal (a DC voltage level) goes to the Interface Board, where it is digitized and read out serially to the 1553 monitoring system. The reading from each RTD is interlocked so that if the temperature goes above 15C, the power to the appropriate HDI (only) is tripped.

In addition to the temperature monitor on each HDI, 88 of these signals have a second readout. An analog signal is taken off the Interface Cards before digitization and read out through an ADC in the DØ Cryo Control System, which is a Programmable Controller (PLC), a commercial system widely used in industry for monitoring and interlocks. The 88 RTDs read out in this way serve as one of several signals that interlock power to the entire silicon system. The Cryo Control System serves as a redundant system to the 1553 interlocks, and is on a UPS so it would still function in the case of a power outage.

7.2.2 Run IIb Temperature Monitoring

In Run IIb there will also be two somewhat redundant temperature-monitoring systems. The system that interlocks the current in each HDI will be reproduced. For Run IIb the HDIs are replaced by hybrids. Each hybrid will have an RTD mounted as one of the elements. Plans and costs for these devices are part of the hybrid design and budget. The devices chosen are Honeywell HEL-700 1000 Ω platinum thin-film RTDs. Signals from each of these RTDs will be digitized on the Interface Card and read out through the 1553 as is currently done for Run IIa. The temperature monitors on each hybrid will be used to interlock the power of that individual hybrid.

For Run IIb, there will be a second temperature-monitoring system which will be decoupled from the hybrids. There will be on order 100 RTDs mounted at various locations on the sensors and cooling system. Each RTD will be mounted on low-mass quad-lead 4-wire ribbon cables with polyimide insulation, which is known to have good rad-hard properties. The cable will extend to the “horseshoe” area, where the low mass cables will be coupled through simple junction cards to high-mass cables which then go to standard RTD readout modules in the DØ

Cryo Control System. A commercially-available module, the CTI505, model 2557-SPQ334, from Control Technology Incorporated, will be used to both provide current to the RTDs and readout the resulting voltages. These modules have been used often at Fermilab. This system will provide an independent set of interlocks on the silicon temperature. The CTI505 modules allow either two or four wire readout and therefore can provide for more accurate monitoring than was available for the Run IIa system. We plan to use the four-wire readout to have more accurate temperature information for these 100 RTDs.

There are several reasons that a second, independent temperature monitoring system is needed in Run IIb. In L0 the hybrids will not be located near the actual sensors. Therefore, for L0, the temperatures of the hybrids, not the sensors themselves, will be monitored with the 1553 system. It is desirable to have additional monitoring which measures the temperatures of the sensors themselves. The stand-alone system will measure the temperature of the sensors, or perhaps the cooling channels nearby. For layers outside of L0, the RTDs mounted on the hybrids also do not directly monitor the temperatures of the sensors, although they are nearby. Additional temperature sensors, mounted either directly on the sensors or on the nearby cooling channels, will provide supplemental information and interlock capability for the outer layers. This capability could be especially important for L1, for which preliminary designs indicate the cooling may be most difficult. Improved accuracy on some subset of the RTDs would allow for improved understanding the cooling system. It is desirable to be able to measure, for example, the difference between the input and output temperatures of the cooling system, but the current temperature readouts are not accurate enough to measure such a small temperature difference. The additional RTDs will be read out via a 4-wire system that compensates for lead resistance and therefore will be more accurate and uniform. Finally, in a system as vulnerable to damage from over-temperature as the silicon detector, redundancy in the interlock system is an advantage if not a requirement.

8 SOFTWARE

This section describes online and offline software needed for SMT commissioning and online calibration, monitoring and readout of the detector. For both offline and online software effort, we will use the system developed for Run IIa and upgrade it appropriately for Run IIb where needed. Here we describe this system.

8.1 Online Software Components

The software requirements are mainly determined by the hardware that is used. The SVX amplifier chip requires a set of parameters like the amplifier bandwidth, a threshold for zero suppression and various ADC settings. The delay for the readout is set at the Sequencer Controller module. Each module requires an individual set of parameters. These parameters are downloaded after power up. Special data taking modes, e.g. calibration runs, require a different set of parameters. In addition some parameters might change with time. The most important example is the threshold for zero suppression, which changes with fluctuations of pedestal and noise. Constant monitoring ensures that the download parameters are still correct. Monitoring is also necessary for ensuring a constant high data quality and the safety of the detector.

The main components of the SMT online software are the ORACLE database, Graphical User Interfaces for control and monitoring, the Secondary Data Acquisition for calibration and monitoring, and Examine programs, which are part of the offline framework but are used in the online context.

8.1.1 The Oracle Database

The Online Database for SMT consists of three parts, the Hardware Database, the Electronics Database and the Online Calibration Database. The Hardware Database contains the definition of EPICS process variables (see below). These are required for communication with hardware modules. In addition alarm information is stored which is used for monitoring and the Significant Event System (SES). The Electronics Database contains the complete mapping of the hardware. Every type of readout module has its own table. An individual module is represented by a row in this table. A representation of single channels of modules allows the necessary multiple to multiple references between readout modules. The database contains the hardware identification for the modules as well as all the parameters necessary to operate the module. A history mechanism allows keeping track of changes to download parameters. This retains a history of the parameters that have been used at any time during the data taking period. The Online Calibration Database contains the basic calibration data for each readout channel per calibration run as well as summary information per SVX chip per calibration run. In addition a status word is assigned to each of the readout channels. These databases are implemented using ORACLE, which is software maintained by the computing division at Fermilab.

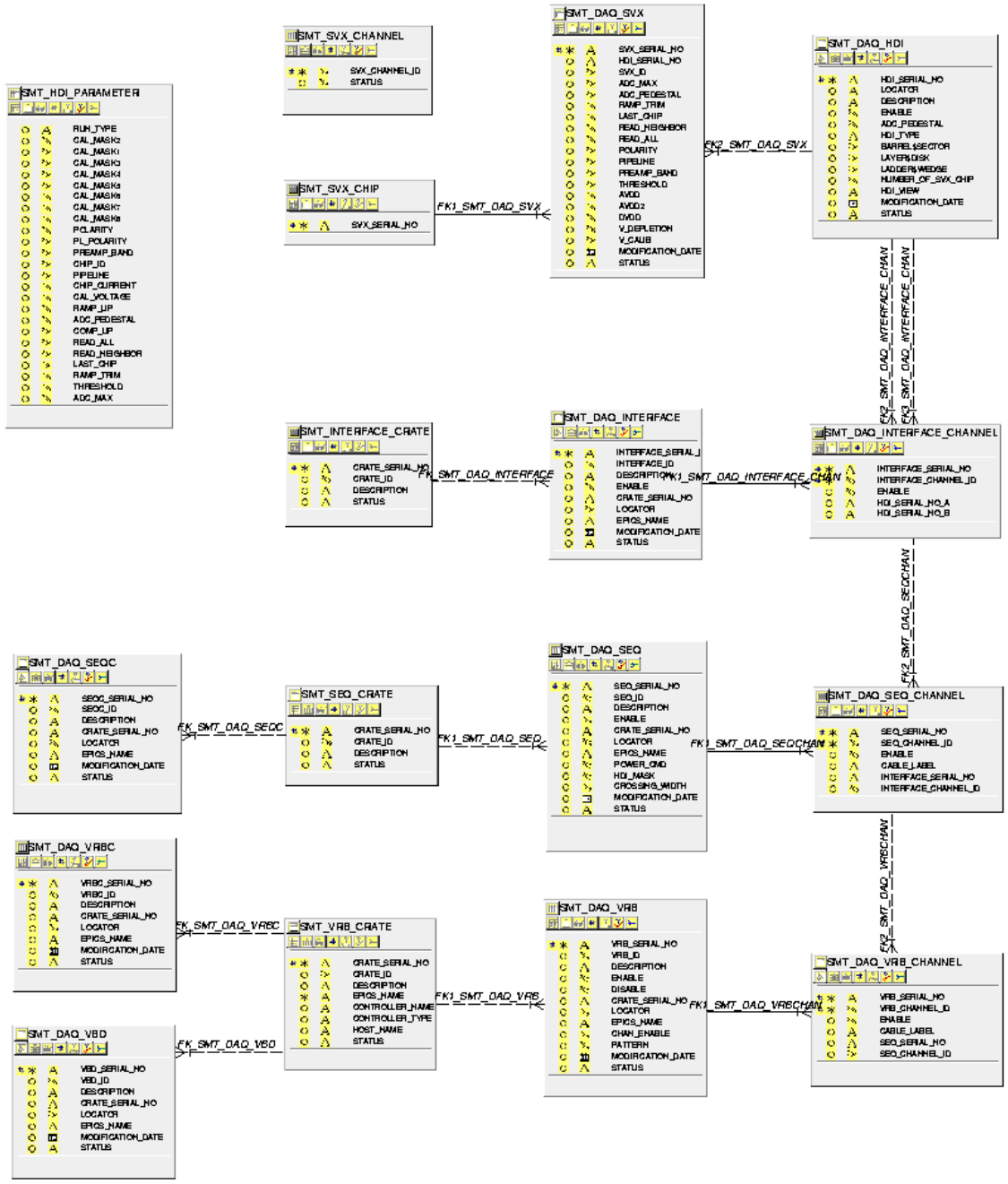


Figure 150 - Entity Relationship Diagram of the Electronics Database. A table represents each module type. The implementation of channel tables allows multiple to multiple relationships.

8.1.2 Graphical User Interfaces

The Graphical User Interfaces (GUIs) include EPICS as well as other control and monitoring interfaces. EPICS (Experimental Physics and Industrial Control System) is used to communicate with the hardware. An Input/Output Controller (IOC), a VME single board computer of the Power PC mv23xx series, maintains a database of symbolic names, which are mapped to one or more hardware addresses. A host computer can access these symbolic names via an EPICS client. EPICS client and server communicate via the Ethernet network. This system allows an easy implementation of a centralized controls and monitoring system with distributed hardware.

The MIL1553 standard is used to communicate with non-VME modules. A custom built VME module, the 1553 Controller, is used to access the 1553 bus. The 1553 bus is a robust communication link widely used in commercial and military aircraft. EPICS is used to communicate with 1553 devices.

EPICS allows periodic sampling of the hardware. Threshold values are used to issue warning or error messages to the Significant Event System (SES). This allows a distributed monitoring of variables locally without the need for a central host. In principle it is possible to implement an immediate response to a monitor value that exceeds a set limit directly on the local machine. The shift crew regularly monitors messages of the SES. These messages are archived as well.

The programming language used to interface the database and the hardware is Python. Python has several advantages:

- Python is an Object Oriented Language. It therefore allows the use of modern programming techniques.
- Python is a script language. It is compiled to a compact, byte-oriented stream for efficient execution. Program development has fast turn around cycles.
- Python has a convenient to use Tcl/Tk library. The programming of Graphical User Interfaces (GUI) is simple and fast.
- Python also has a freely available interface to ORACLE databases.
- A Python wrapper around the C-interface to EPICS has been developed by DØ.

Because of those advantages Python has been the choice to develop GUIs for interaction with the database and with the hardware. One of the few disadvantages is that the execution speed is not as fast as for example a ‘C’ program could be.

A GUI, the so-called Download GUI, has been developed to interface both the ORACLE database and the hardware. The database is used to determine the mapping of the readout electronics. Each module is represented by one GUI entity. Each entity has two functionalities:

- The parameters for a specific module that are stored in the database can be modified.
- The hardware registers of this module can be accessed.

Specifically it allows operations on the following list of hardware (the complete list of operations is given later in this chapter under 8.3 Hardware Operations.

- VRB
- VRB Controller
- Sequencer
- Sequencer Controller
- KSU Interface Board
- HDI
- VRB Crate
- VBD

Additional GUIs are available for:

- Monitoring of voltages, currents and temperatures of all the HDIs. The KSU Interface Board is used to determine these parameters. Most commonly the value of the DVDD current and color-coded status information (on, off, limit exceeded trip) is displayed. The protection against over current or over temperature is implemented in hardware in the KSU Interface Board.
- Monitoring and Control of the bias voltage of the silicon. Each silicon detector has one or two bias voltages that have to be set individually. Characteristic values are: trip voltage, which is set as hardware limit at the HV module itself, maximum current, nominal voltage, lower/higher minor/major alarm limits for voltages and currents, and the ramping time constant. These values are stored in an ORACLE database. If one of the predefined limits is exceeded an alarm is sent to the Significant Event System. Two different GUIs allow the manipulation of the HV system.
- Monitoring of temperatures of the Interface Boards. Six channels of the KSU Interface Board per crate are used to read the temperature of the cooling air for those crates. The result is displayed in a separate GUI. The crate is switched off if more than 2 temperature read backs exceed a given limit.
- Monitoring and Control of the low voltage power supplies. There is one GUI each for the power supply of the KSU Interface Boards and for the power supply of the sequencers. Voltages and currents are monitored and alarm messages are sent to the Significant Event System in case that limits are exceeded. The GUIs also provide the possibility to switch power on and off and to reset trips.
- Monitoring and Control of the VME single board computers. CPU usage, memory usage and the number of used file descriptors are monitored for all of the IOCs. Alarm limits are set for the Significant Event System. The GUI allows the user as well to reboot any IOC remotely.
- Security monitoring. Environmental variables of electronic racks are monitored using the Rack Monitor. Monitored parameters are airflow, smoke detection, water flow and water drip. The rack power and air blower are interlocked with any of these parameters in hardware. If a water drip is detected the water flow is switched off. An alarm message is sent to the Significant Event System if a trip is detected. A GUI allows to monitor the environmental parameters and to reset a trip.

Any EPICS variable can be read out with a frequency of up to 10Hz. For archiving purposes the following quantities are read out once per minute:

- Silicon ambient temperature
- Cooling water input/output temperature
- Count rate of the SMT radiation monitor fingers
- Voltage and temperature of the high voltage power supplies
- Voltage, current and temperature of the sequencer power supplies
- Voltage, current, temperature and magnetic field of the KSU Interface Board power supplies (rate 1Hz)
- Voltage and current for each HV channel
- Voltage, current and temperature of each of the HDIs

This data is stored on disk and on a weekly basis transferred to SAM for permanent archiving. Two other tools allow working with that data: The Strip Tools can display a strip chart of any EPICS variable online. Data that has already been archived in a file can be displayed using the Channel Archiver GUI.

8.1.3 Secondary Data Acquisition

The calibration of the silicon detectors is done using the Secondary Data Acquisition (SDAQ) system. SDAQ is integrated in the DØ DAQ framework (see Figure 151). The Coordinator Process (COOR) hands control over to the Calibration Manager when the shifter requests a calibration run. The SDAQ Supervisor receives a list of crates that are configured for the calibration run. The Input/Output Controller (IOC) of each crate receives the request for a calibration run together with all configuration parameters necessary for its execution.

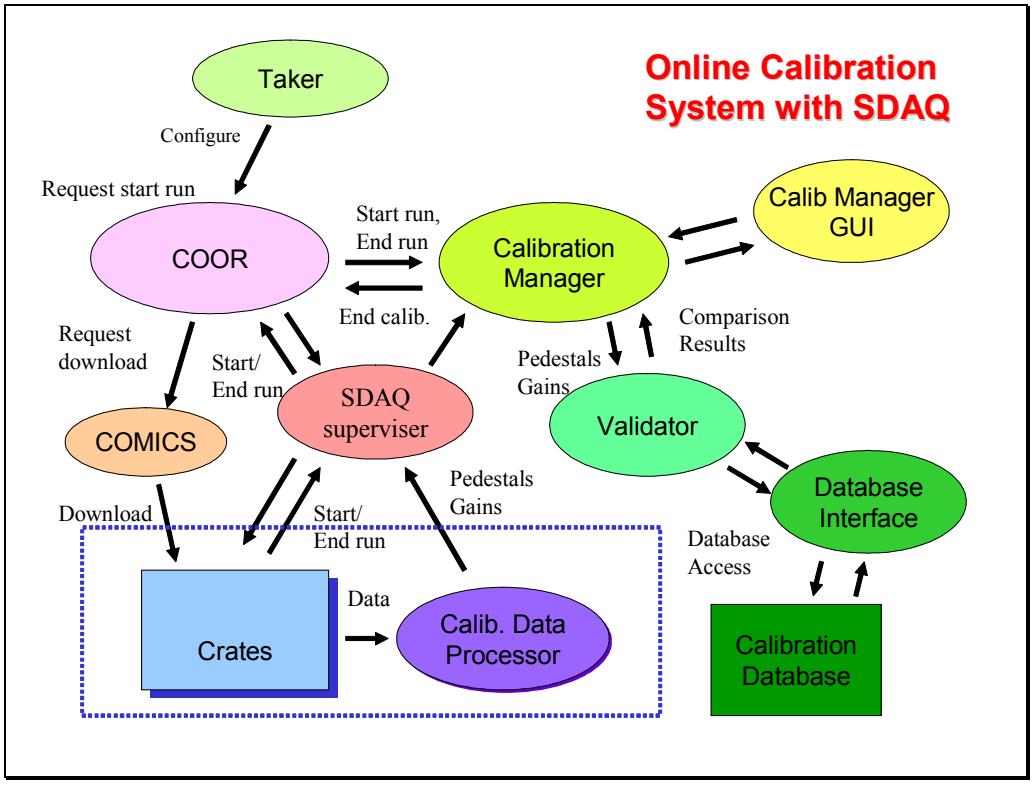


Figure 151- Relationship between different processes in the Online Calibration System. The Calibration Manager is the central part of this system. The calibration result is stored in the Calibration Database.

The operating system used on the IOC is VxWorks. VxWorks is a real time operating system that is supported by Fermilab. The code running on the IOC has been programmed in C for Run IIa. Each IOC performs its task independent thus parallelizing the calibration process. The IOC does the following:

1. Triggers are inhibited until the initialization process is finished.
2. A predefined set of channels to be calibrated is downloaded into the SVX chips. The SVX chips are set into "read all mode", i.e. zero suppression is switched off.
3. The VRB Controller (VRBC) is set into SDAQ mode. It is configured to send interrupts for each L1 trigger after the data has been received. A larger buffer size for the VRBs is selected as the data size exceeds the regular buffer size that is used when zero suppression is active.
4. DMA transfer on the VME bus is initialized for all VRBs.
5. The desired calibration voltage is set at the Sequencers. The calibration voltage is changed to predefined values in case a gain run is requested. Typically 5 different calibration voltages are chosen for each of the two different chip polarities.
6. The inhibit signal to the trigger framework is cleared.

The Trigger Framework sends regular L1 Triggers to all crates participating in the calibration run. The data is collected in the usual way (see Figure 94): The Sequencer Controllers and the VRB Controllers receive the L1 triggers. The SVX data is read out and stored in the VRBs. The calibration run requires a L2 reject for each given L1 trigger in contrast to the normal data taking mode. In this way the data is processed locally in the crate processor and is not sent to the L3 farm. The VRBC prepares the VRBs to be read out and sends an interrupt on the VME bus. The IOC catches this signal and a VME 64-bit DMA transfer from all VRBs is initiated. The IOC processes the data:

1. Additional triggers are inhibited while the data is being processed.
2. The data is decoded to get information about each strip.
3. Basic error checking is performed.
4. The number of events, the sum of the data values and the sum of the squares are stored per strip.

Typically 800 events are collected for a calibration run. The mean and r.m.s. of the collected data is calculated for each calibration voltage setting. In case of a gain run a two parameter fit to the data is performed. The final result per strip is the pedestal value, the r.m.s. of the pedestal, the slope of the fitted line, the uncertainty on the slope, and an error flag. This result is sent to the Calibration Manager. The Validator can perform a simple data integrity check. Approved data is finally stored in the Calibration Database.

A separate process uses this information to calculate significant parameters for each readout chip. Each SVX readout chip requires a single threshold for zero suppression. The new threshold is chosen to be the average pedestal of the 128 readout channels plus 6 ADC counts. The typical pedestal r.m.s is about 2 ADC counts so that the threshold is 3 r.m.s above the pedestal level. Figure 152 shows the calibration result for an HDI as example. Several checks are performed on this result:

- The new threshold should not differ by more than 5 ADC counts from the previous threshold. Experience shows that pedestal levels change only slowly.
- The number of noisy strips per chip is calculated. An HDI is marked as problematic if more than 2% of the strips have an ADC count greater than 6. An SVX chip can be masked out if the resulting occupancy is too high.
- A channel is suppressed if the pedestal for the channel is more than 25 ADC counts below threshold. An HDI is marked as problematic if more than 2% of its channels are suppressed.

In case a problem is detected human intervention is required. A GUI that displays the calibration result and gives the user the possibility to manipulate the data exists. The final new threshold can be used as download parameter for the next data taking period.

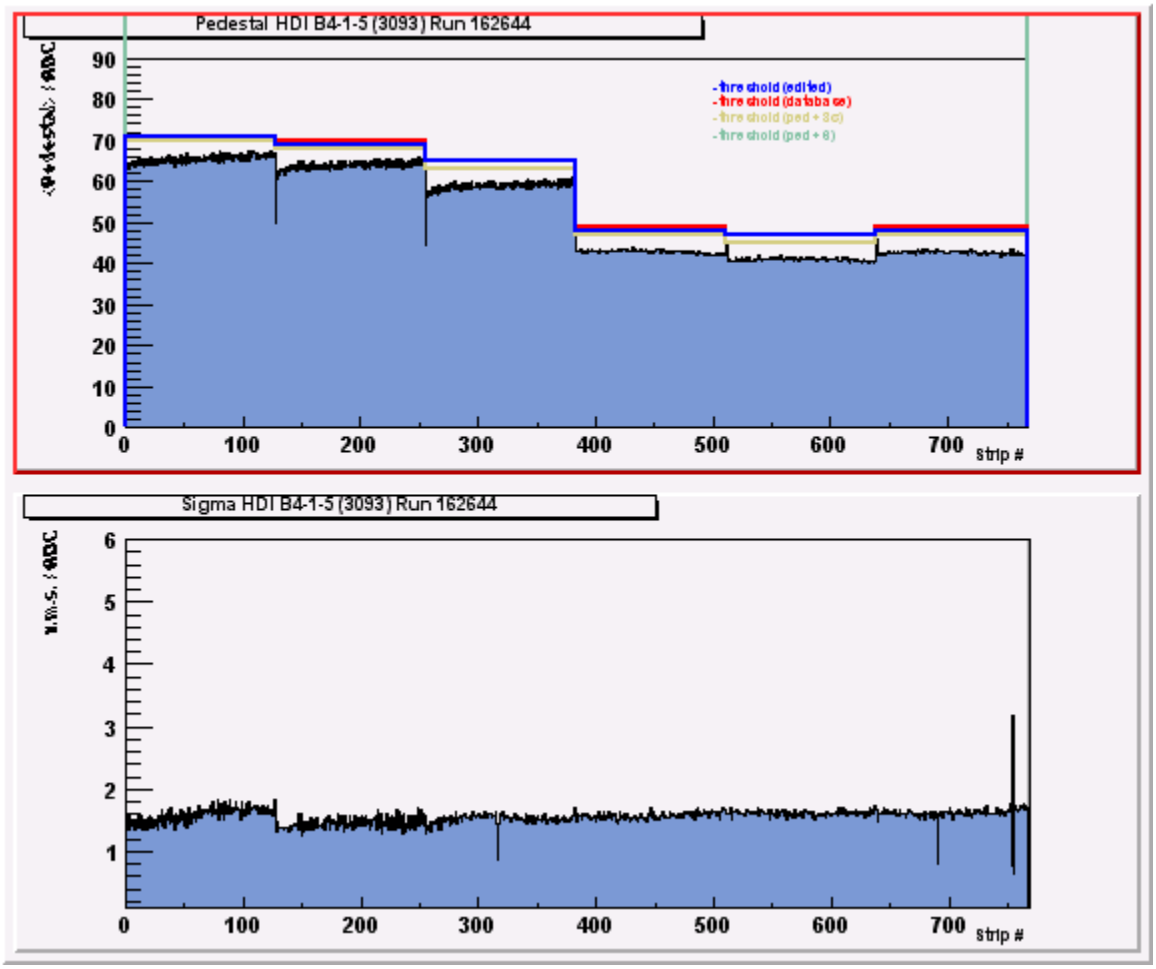


Figure 152 - Calibration result for HDI B4-1-5. The upper histogram shows the mean value of the pedestal distribution after 800 events in ADC counts versus the strip number within the HDI. The red line marks the valid threshold that is in the database at the moment.

8.1.4 Run IIb Modifications

The same calibration system will be used in Run IIb. As the readout system downstream of the Sequencer is identical only minor changes will be necessary. We will need to update the ORACLE database to accommodate the new active adaptor cards. The population of the database was done starting from an EXCEL spreadsheet. Visual Basic scripts were used to extract the information and fill the database. This work will need to be done again. The only other concern is the fine tuning of the download timing. As a new generation of readout chips will be employed, timing requirements may be different. These will need to be tuned.

8.1.5 Data Monitoring During Runs

The same SDAQ program is also used for monitoring while a normal Primary Data Acquisition (PDAQ) run is ongoing. Several data transfer modes are possible:

- The IOC catches an interrupt sent by the VRBC when the data is available. A prescale can be set to adjust the rate of monitor events. The IOC reads the data from an internal Monitor FIFO of the VRB, the so-called Spy Memory. As this memory area can only be accessed by single word read operations, the data transfer is rather slow. Eight different VRB channels share one Spy memory so that only 1/8 of an event can be read.
- The 8KByte large FIFO can also be read out through an auxiliary port. For the time being only the VME readout is implemented but alternate readout schemes like IEEE1394 are under consideration for this.
- The IOC reads the data from the regular VRB memory. This procedure can introduce additional dead time while the VRB is read out.
- The IOC reads data from the Single Board Computer (SBC), the module that replaced the VBD as L3 Trigger interface. In this case a fast VME 64-bit transfer can be used, utilizing spare bandwidth of the VME backplane.

The data is collected and analyzed by the IOC, which sends analyzed data to a LINUX host computer. A three-threaded monitoring application is running on this machine:

1. One thread collects data from all IOCs via TCP IP sockets and stores them in a global data structure. This global data structure is modeled after the hardware configuration of crates, VRBs, HDIs and chips as defined by the ORACLE database. It contains information about signals, hit distributions, occupancy and errors for all HDIs and chips.
2. The second thread serves data to Java Servlets (TCP IP sockets) that are used to display histograms on a WWW browser.
3. The third thread is used to check data every 10000 events and sends information about dead or faulty hardware or high occupancy HDIs to the Significant Event System.

All common data structures shared by the threads are synchronized by a set of semaphores. The Java Servlets allow querying for:

- Dead hardware: HDIs are marked dead when a readout chip gives no signals.
- Faulty hardware: HDIs are marked faulty when a previously working channel gives no signal.
- Occupancy: Contains the occupancy distribution for HDIs and chips.
- Data signal: Distribution of mean values of all signals per HDI or SVX.
- Hit count: Hit count per SVX and per readout channel. An example is shown in Figure 153.
- Errors: Errors detected in the collected data (missing strips, wrong chip id, channel ordering error).

The servlets generate output in a text mode and a graphics mode. Histograms are created using the free product JPGraph written in PHP.

Observing the occupancy allows monitoring when a new threshold for zero suppression needs to be determined. A message is sent to the Significant Event System if the occupancy reaches a predefined limit.

The offline monitoring with "Examine" processes allows full reconstruction of a small number of events. Apart from occupancy histograms this allows a SMT specific event display, Landau distributions of clusters and the reconstruction of tracks and vertices.

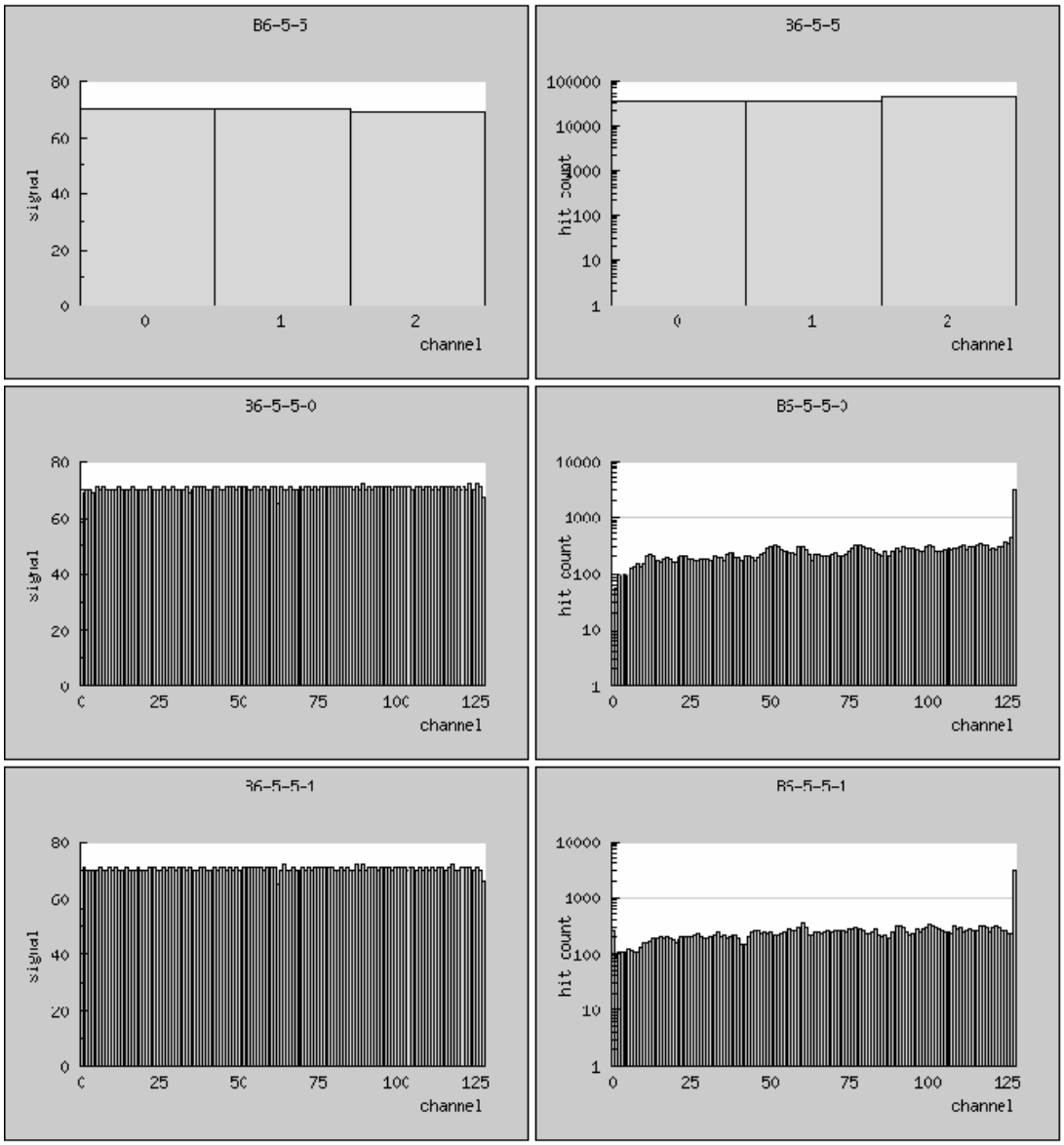


Figure 153- Graphs produced with the Online Monitoring: Hits per SVX chip (upper row) and hits versus channel number (middle and lower row).

8.2 Offline software

SMT commissioning and tests of SMT detector sectors during the production using the realistic readout chain require software tools for online and offline analysis of silicon data. In Run IIa SMT Examine package produces a variety of histograms for each SMT detector element that allow study pedestal distributions, total, correlated and random noise, occupancies and cluster charge and size distributions. SMT Event Display provides a visual representation of fired channels and reconstructed hits in silicon. Both packages use as input the data collected through the primary data path and can run in offline as well as online modes. The corresponding data flow chart along with the Run IIa software packages is presented in Figure 154. In offline mode analysis packages read raw data file produced by Level 3 trigger framework. In online one data from Level 3 is transferred to the Data collector, which passes it to Data distributor. Data distributor delivers data to different clients and ultimately to SMT Examine and SMT Event Display. The same data processing path will be used in Run IIb.

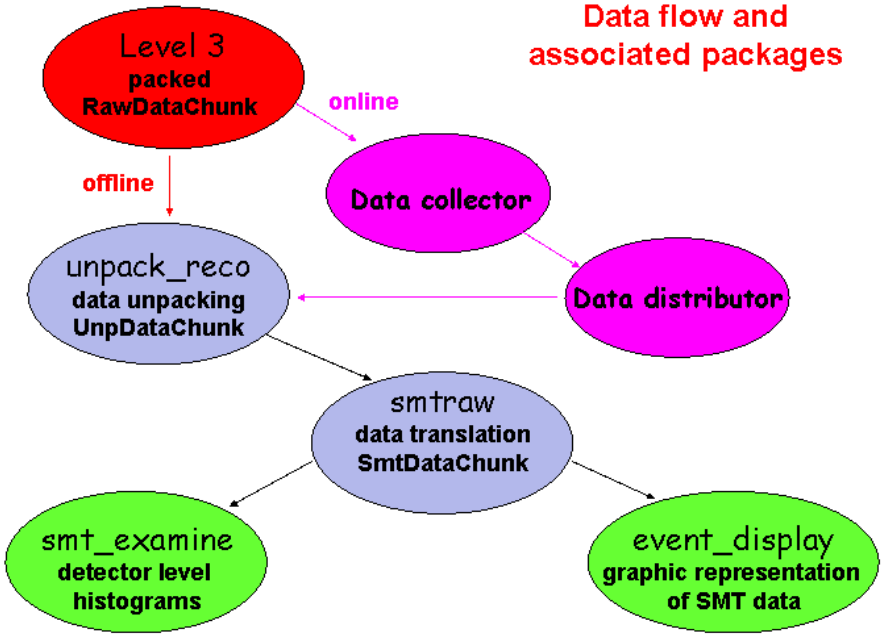


Figure 154 - Primary data acquisition data flow diagram with associated packages for online and offline modes of running SMT Examine and SMT Event Display.

To minimize the storage space and network transfer time data coming out of Level 3 is packed. The packing format is defined mainly by the hardware used in the SMT readout chain. Since as mentioned above the readout system downstream of the Sequencer is identical to the one of Run IIa, no major changes are expected in the packed data format and therefore only minor changes will be needed to the SMT data unpacking package.

Data unpacking is followed in the data processing chain by the package responsible for the translation of electronic addresses of SMT elements into the physics addresses. This translation

is based on the cabling scheme of the SMT detector, which will be replaced to match Run IIb SMT design. Significant modifications of the translation package will be required to accommodate these changes. The same is true for SMT Examine and SMT Event Display packages which also heavily depend on the SMT design.

8.3 Hardware Operations

In the following interactions with the different hardware modules are described. The actual values for the download are extracted from the database if not stated otherwise.

8.3.1 VRB

- reset: Issues a reset.
- init: Initializes the channel selection, simulation mode and Grey decoding registers.
- j3enable/j3disable: Enables/disables communication via the custom made part of the backplane
- chan disable: Disables all VRB input channels.
- sim data: Switches to auto generated data.
- conf buffer: Configures the VRB buffers.
- print register: Prints all status registers.

8.3.2 SEQ

- download: Downloads all SVX chips connected to this Sequencer.
- HDI off: Sets the HDI enable bits to 0. The effect is that the low voltage to the SVX chips is switched off.
- complete init: Downloads all SVX chips and initializes the sequencer
- init: Initializes the sequencer only.
- reset: Sends a reset command to the sequencer.
- set cxpw: Sets the crossing pulse width.
- set calv: Sets the calibration voltage.
- set calv 0: Sets the calibration voltage to zero.
- set hdim: Sets the HDI mask. This bit pattern allows ignoring certain input channels.
- set powr: Sets the power/hdi enable bit for each channel
- power on: Sets the power/hdi enable bits for all channels to 1.
- print temp: Prints the temperature as measured by the upper most optical transmitter.
- print status: Prints the 1553 status word. Should be 0 if the last transmission was correct.
- print CALV: Prints the value of the calibration voltage currently set.
- print HV status: Prints the status of the HV for all HDIs of this sequencer (On, Off, Locked, Tripped, Disabled).

8.3.3 SEQ channel

- download: Downloads the two HDIs connected to this sequencer channel.
- power off: Sets the HDI enable bits for those two HDIs to 0.
- set nch: Sets the number of SVX chips for the HDIs.
- check hdis: Compares the read back of the SVX configuration with the download value.
- print HV status: Prints the status of the HV for those two HDIs.
- print SVX read back: Prints the read back of the SVX download string as series of hex numbers.

8.3.4 KSU Interface board (INT)

- start HV GUI: Starts HV GUI for the HDIs connected to this Interface Board.
- start IB GUI: Starts the IB GUI for those HDIs. This GUI display the voltage, current and temperature information as read by the KSU Interface Board.

8.3.5 HDI

- power off: Sets the HDI enable bit for this HDI to 0.
- print HV pods: Lists the HV pods for this HDI.
- print HV status: Prints the HV status for this HDI.
- HV pods GUI: Starts the HV GUI for HV pods connected to this HDI.
- SVX GUI: Starts a GUI that allows changing individual SVX download parameters.
- SVX Thresholds: Starts a GUI that displays the Thresholds of the last ten calibration runs for all SVX of this HDI. This GUI allows a simple manipulation of threshold values for the next download.

In addition to providing an interface to single readout modules, global functions acting on a complete readout crate are implemented:

8.3.6 VRB Crate (VRBCR):

Operations to all modules of the same type connected to this VRB crate.

- HDI power off: Sets the HDI enable bits to 0 for all sequencers.
- SEQ set CALV: Sets the calibration voltage on all sequencers.
- SEQ CALV 0: Sets the calibration voltage on all sequencers to 0.
- SEQ set CXPW: Sets the crossing pulse width on all sequencers.
- VRB reset: Resets all VRBs
- VRB init: Initializes all VRBs
- VRB enable: Tells the database and the GUI to use all VRBs.
- VRB disable: Tells the database and the GUI to ignore all VRBs.
- VRB j3enable: Sets the j3enable for all VRBs.

- VRB j3disable: Sets the j3disable for all VRBs.
- VRB j3default: Sets the j3enable bit according to the database enable information.
- VRB pattern: Switches all VRBs into auto generated data mode.
- VRB no pattern: Switches all VRBs back to normal data taking mode.
- VRB print reg: Prints the register content of all VRBs.
- scan HV: Scans the HV status of all HDIs. The result is displays in different color codes.
- start HV GUI: Starts a HV GUI with all HV channels that are connected to HDIs in this crate.
- print hdi list: Prints a list of HDIs in this crate.
- write sdaq file: Writes a configuration file containing the current settings that can be read by a sdaq process.
- write mon cal file: Writes a file with calibration database information for online monitoring.
- write off cal file: Writes a file with the most recent calibration information for examine and offline processes.
- write pickle file: Writes a file with download information for COMICS.
- write transl map: Writes a file with the latest translation map between VRB channels and HDIs.

8.3.7 VRB Controller (VRBC)

- init: Initializes the VRBC.
- reset: Sends reset command to the VRBC.
- 53 MHz: Switches internal 53 MHz oscillator of the VRBC on.
- idle mode: Switches the internal NRZ generator into idle mode.
- acquire mode: Switches the internal NRZ generator into acquire mode.
- PDAQ mode: Switches the VRBC into PDAQ mode.
- SDAQ mode: Switches the VRBC into SDAQ mode.
- P+SDAQ mode: Switches the VRBC into PDAQ monitoring mode.
- 16x2K buffer: Selects the 16 buffers of the VRB of 2K size.
- 8x4K buffer: Selects the 8 buffers of the VRB of 4K size. The physical memory is actually the same, the address space is configured differently.
- send trigger: Sends a trigger command to the VRBC.
- cal inject: Sends a trigger command to the VRBC and causes a NRZ calibration pulse code to be generated.
- N cal inject: Sends N=10 cal inject commands.
- print SCL status: Prints the contents of the SCL status register.
- print mode: Prints the current mode information of the VRBC.

8.3.8 VRB Buffer Driver (VBD).

The VBD has been replaced with a Single Board Computer (SBC). However, the SBC emulates the VBD and has therefore the same register structure.

- init: Initializes the VBD.
- clear memory: Clears the VBD memory.
- use VME: Tells the VBD to use the VME backplane for data transfer.
- read evt len: Reads the event length information from the VBD.
- read event: Reads a complete event from the VBD. The result is displayed graphically in a separate GUI window.
- print crate type: Prints the crate type information.
- print event address: Prints the register containing the event address.
- print status: Prints the status register.

8.3.9 Sequencer Controller (SEQC)

- reset: Sends a reset command.
- init: Initializes the SEQC.
- delay: Sets the delay registers.
- set rdo abort: Switches the readout abort feature on. In this mode the readout is aborted after 3.5μs.
- clr rdo abort: Switches the readout abort feature off.
- use SCL: Switches the SEQC into SCL mode.
- use 1553: Switches the SEQC into 1553 mode.
- use SCL Cal: Switches the SEQC into SCL mode. For each L1 Trigger a calibration pulse is issued. This mode is used for gain calibration runs.
- idle mode: Switches the SEQC into idle mode for download.
- acquire mode: Switches the SEQC into acquire mode for data taking.
- cal inject: Sends a trigger command to the SEQC. A calibration pulse is injected into the SVX.
- N cal inject: Sends N=10 cal inject commands.
- print status: Prints the status registers.

8.3.10 Global options

- download: Complete initialization of all modules connected to this crate is performed.
- HDIs off: Switch all HDIs in this crate off.
- cal inject: Generation, recording and displaying of a pedestal or pulser event.
- reinit VME: Reinitialize all VRBs, the VRBC, VBD and SEQC connected to this crate.
- calibration:
    - Process Pedestal Run: Processes a calibration run and calculates new thresholds.
    - Process Gain Run: Processes a gain run and determines potentially dead strips.
    - Print Stat all Runs: Prints a summary of the last 10 calibration runs for this crate.
    - Print Stat one Run: Prints a summary of the last calibration run.
    - Select new threshold: Starts a GUI that allows the selection of a new threshold for zero suppression for the next download.

The status registers of all the modules are polled with a predefined frequency. The result of this poll is displayed in the GUI as different color codes. The following colors are used:

- Grey: Status is unknown.
- Orange: Power is off.
- White: The module is not usable.
- Yellow: The module is disabled.
- Green: OK.
- Sea green: The module is OK but not in its standard configuration.
- Magenta: The module needs to be updated.
- Red: The module returns an error status.

9 SIMULATION OF THE SILICON DETECTOR PERFORMANCE FOR RUN IIB

9.1 Overview

The DØ Run IIb group performed a detailed simulation of the Run IIb silicon microstrip tracker. The simulation included a full Geant simulation of the underlying physical process, data-tuned models of detector response, and complete reconstruction of simulated events, including pattern recognition, within the DØ Run IIb software framework. Quantitative calculations of occupancy, impact parameter resolution, momentum resolution, and b-quark tagging efficiency verify substantial improvements in performance over the presently operating Run IIa silicon detector. These full Geant results are presented below.

9.2 Silicon Geometry in the Simulation

The Run IIb silicon detector is modeled as a barrel tracker consisting of six concentric cylindrical layers, numbered from 0 to 5 in going from the innermost radius of 19 mm to the outermost radius of 164 mm, respectively. Pseudorapidity coverage extends from -2.5 to +2.5. Each layer consists of two sub-layers that preserve a six-fold symmetry for the silicon track trigger. Layers 0 and 1 were simulated with axial silicon detectors only, while layers 2 through 5 contained axial-stereo pairs of single-sided detectors in each sub-layer. Figure 155 shows an *x-y* view of the Run IIb silicon detector geometry as implemented in the simulations, Figure 156 shows an x-z view, and Table 27 gives positions, dimensions, and stereo angles of the detector modules used for this work.

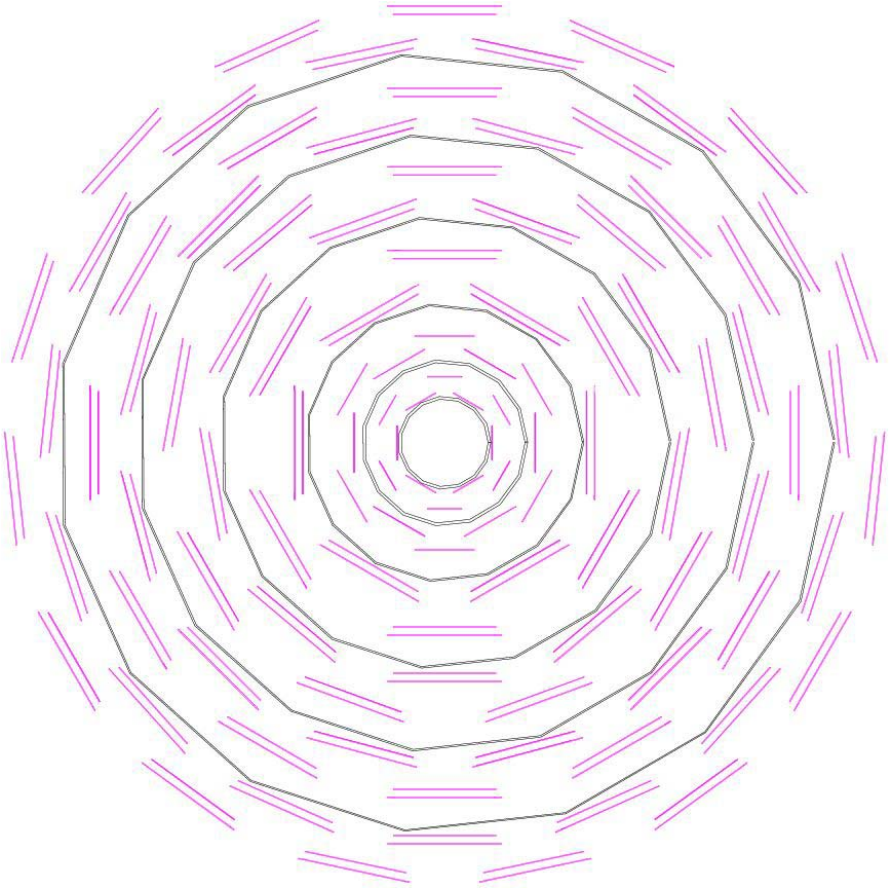


Figure 155 - Geometric layout used in the Geant simulation of Run IIb silicon detector.

Figure 156 An xz view of the Run IIb detector as implemented in the Geant simulation.

Table 27 - Parameters of the Run IIb silicon tracker used in the GEANT simulation.

Layer	*Radius (cm)*	*# of sensors in z*	*Sensor Length (cm)*	*Sensor Pitch (μm)*	*Stereo angle (degrees)*
0a, 0b	1.780 / 2.465	12	7.94	50	0 / 0
1a, 1b	3.400 / 4.000	10	7.84	58	0 / 0
2a, 2b	5.478 / 7.048	10	10.0	60	±2.5 / ±1.25
3a, 3b	8.781 / 10.183	10	10.0	60	±2.5 / ±1.25
4a, 4b	11.848 / 13.112	12	10.0	60	±2.5 / ±1.25
5a, 5b	14.853 / 16.204	12	10.0	60	±2.5 / ±1.25

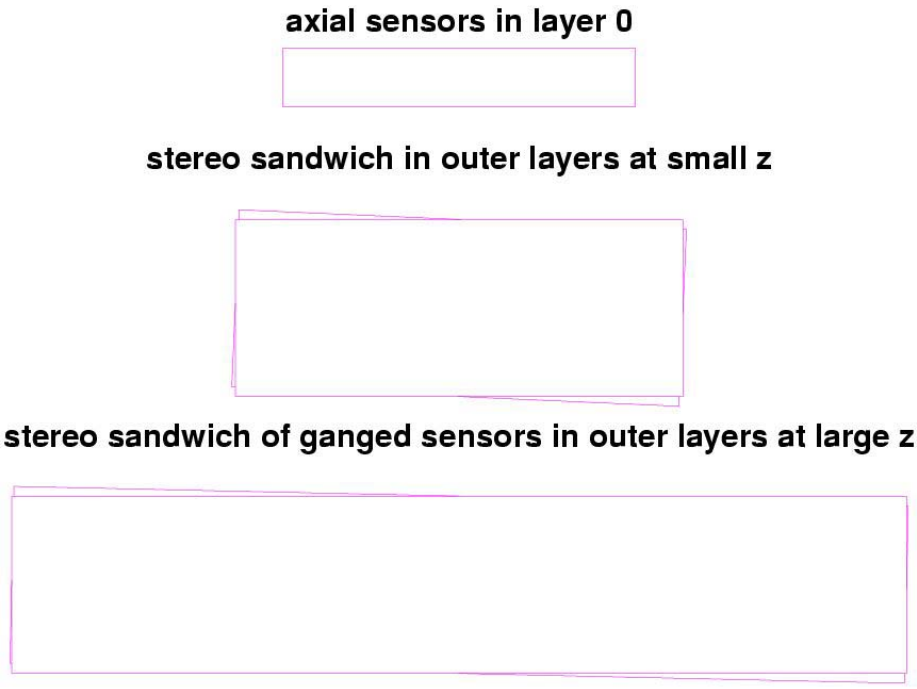


Figure 157 - Layout of axial and axial-stereo modules.

Barrel modules[34] are assembled end-to-end on long staves placed on carbon fiber support cylinders that lie parallel to the z-axis of the detector. Staves hold six modules each in layers 0-1 and four modules in layers 2-5. The design of the Run IIb silicon detector requires two kinds of axial modules and four kinds of axial-stereo "sandwiches". The axial types are simulated as silicon plates of 1.55 or 2.4972 cm width (depending on layer, layer 0 has narrow detectors and layer 1 has wider detectors), 7.94 cm length and 300 μm thickness. The design of the Run IIb silicon detector requires axial modules and two kinds of axial-stereo “sandwiches”. The axial

[34] “Module” here refers to a geometric unit used in the Geant simulation. Readout modules may be different.

type is simulated as a silicon plate of 1.48 cm width, 7.84 cm length and 300 μm thickness[35]. A sandwich silicon module consists of two equivalent silicon sensors, one axially oriented and the other rotated with respect to the beam axis. The radial distance between the two silicon planes in the sandwich is 3.094 mm, and the angle of the rotation is ±2.5 degrees for the small sandwiches and ±1.25 degrees for the stereo pairs of ganged detectors. The size of the silicon ladders in the sandwiches is 4.11 cm × 10 cm × 300 μm. Axial and stereo modules are shown in Figure 157.

All studies assume a functioning CFT in Run IIb. Thus, a central track can have up to 14 hits—six in the SMT and eight in the CFT. The new layer 0 becomes the innermost hit on the track, and the new layer 5 is the sixth of fourteen hits.

Low mass readout cables are modeled as copper plates of 1 cm width that go out of the edge of first and third silicon modules in every layer.

9.3 Simulation of Signal, Digitization and Cluster Reconstruction

Geant simulates hits in the silicon sensors, and a modified DØ Run IIa package DØSim[36] package digitizes signals.

Input for DØSim consists of a bank of GEANT hits, each of which is described by entry/exit positions and energy deposition in the silicon. Silicon *dE/dx* is simulated via explicit generation of δ-rays that resulted in a Landau distribution of deposited energy. No additional fluctuations in energy loss were considered.

In order to reproduce the effects of ganging sensors together correctly in the readout, hits within ±1.5 mm of the midpoint in z of long axial/stereo sandwich modules were discarded at the digitization step.

The total deposited energy is converted into the number of electron-hole pairs using a coefficient C=2.778×10^8 GeV^{-1}. Charge collection on strips is computed from a diffusion model with the standard drift and Hall mobility of the charge carriers in silicon evaluated at the nominal silicon operating temperature. Charge sharing between strips through intermediate strip wiring is determined by inter-strip capacitance, readout-ground capacitance, and the input capacitance of preamplifier, values of which are taken from Run IIa measurements.

Electronic noise is added to the readout strips after hits have been digitized. Parameters for noise simulation were extracted from the readout electronics noise parameterization and silicon detector prototype studies for Run IIa[37]. This set of parameters leads to a S/N ratio of 16:1, and this value is used for all tracking performance studies. For occupancy studies the average noise was simulated for each channel according to Gaussian distribution with σ=2.1 ADC counts that decreases the signal-to-noise ratio to 10:1, again consistent with the Run IIa data. A similar

[35] The actual sensors turn out to be 320 μm thick.
[36] http://www-d0.fnal.gov/newd0/d0atwork/computing/MonteCarlo/simulation/d0sim.html.
[37] J. Ellison and A. Heinson, "Effects of Radiation Damage on the DØ Silicon Tracker", DØ Note 2679, July, 1995.

signal-to-noise ratio is expected for the end of Run IIb (see the section on sensors). Only those strips above a threshold of 4 ADC counts are saved for cluster reconstruction.

The choice of the threshold for the readout and cluster reconstruction represents a trade-off between efficiency of the cluster reconstruction and noise suppression. Figure 158 shows the probability to read out a strip as a function of strip energy deposition in minimum ionizing particle (MIP) equivalents, and to have a fake hit due to electronic noise as function of the readout threshold. One can see that a readout threshold of 6 ADC counts leads to 20% probability of losing a strip that collects 1/3 MIP while significantly suppressing the noise contribution.

Reconstruction of one-dimensional clusters was performed using a modified package for Run IIa cluster finding. The clusters are defined as a collection of neighbor strips with total charge more than 12 ADC counts. Only those strips registering above 6 ADC counts are allowed in the cluster. The position of the cluster is calculated with a center of mass algorithm independent of the cluster size.

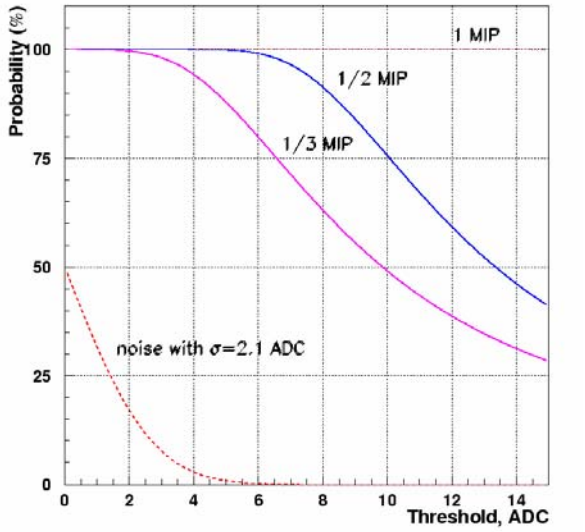


Figure 158 - Probability to have a hit on strip with different fraction of MIP's charge.

9.4 Analysis Tools

Occupancy and position resolution studies utilize a modified Run IIa DØ SmtAnalyze package that allows access to raw and digitized Geant hits and reconstructed clusters. Pattern recognition was performed using the DØ Run IIa Histogramming Track Finder[38] (HTF) modified for Run IIb-specific geometric features. The HTF algorithm is based on pre-selection of hit patterns ("templates") in both the silicon detector and the DØ fiber tracker with particular r-ϕ and z-η properties. Hit patterns are further cleaned and fitted using a standard Kalman filtering technique. The separation of r-ϕ and stereo measuring detectors in the Run IIb silicon detector by

[38] A. Khanov, R. Demina "Histogramming Track Finding Algorithm Performance Study", DØ Note 3845.

a finite gap required modification to HTF as the precise z position of hits could be determined only after the actual track direction was found. After suitable adjustment, HTF demonstrated the good performance seen for Run IIa. All results assume no degradation in fiber tracker performance between Run IIa and Run IIb.

The choice of the non-default DØ tracking package HTF was motivated primarily by the availability of its author to make necessary modifications in the tracking package to handle the changed Run IIb geometry. The tracking code could be adjusted to read out geometries directly from GEANT. HTF has been shown to at least match the performance of the standard DØ tracking package, called GTR, with Run IIa data, with the added benefit that it could be used in a manner decoupled from ongoing Run IIa software development.

9.5 Performance Benchmarks

Basic tracker performance was studied with 2000 event single muon samples generated with transverse momenta of 1, 5, and 50 GeV/c. The primary vertex was fixed in the transverse plane at x=y=0; and z was distributed about zero with a 15 cm Gaussian width.

For estimation of the physics performance, representative signal channels have been chosen and simulated with zero, six, or 7.5 minimum bias (MB) events overlaid. For the latter sample, the pileup events were generated with a Poisson distribution with a mean of 7.5. Minimum bias events were generated in separate runs of Geant. Hits from these samples were combined with those of signal processes at the digitization level. Pattern recognition, track reconstruction in jets, and b-tagging efficiency were studied by examining associated production of Higgs with a W-boson. The Higgs boson mass was chosen to be 120 GeV/c^2, and the Higgs was forced to decay to a bb pair. The W-boson was forced to decay leptonically. Z-boson production followed by decay to light (u or d) quarks was used to estimate the fake rate of the b-tagging algorithm. Minimum bias events were generated with PYTHIA (version 6.2) using a set of parameters tuned to CDF run 1 MB data[39]. Samples of at least 2000 events were processed through the full simulation chain for all studies, with larger samples of 5000 events used for luminosity and occupancy studies.

9.6 Results

9.6.1 Occupancy

Occupancy in the innermost layers is one of the most important issues for the Run IIb silicon detector operation and performance. Four concerns related to occupancy impact the design. The first, radiation damage, limits the lifetime of the sensors; radiation damage and its radial dependence are discussed in detail in the TDR section devoted to sensors. Second is the number of hits per module to be read out per event, which can cause excessive dead time if too large. The relationship between number of hits and charge collection per strip is addressed in the TDR electronics section. Another concern is that a high occupancy in the innermost layer could lead

[39] R. Field, "The Underlying Event in Hard Scattering Processes'', http://fnth31.fnal.gov/runiimc.

to a significant fraction of wide clusters formed by overlapping tracks that may worsen spatial resolution. The occupancy is also an important factor in the pattern recognition.

Occupancy has been studied in detail using the samples of WH events both with and without six additional MB events, and with pure MB events. In all cases, electronic noise was added to physics events. Minimum bias events were used to estimate the average occupancy as a function of radius. Peak occupancies occur in the WH with MB events and were estimated using the WH plus 6MB sample by looking at the silicon module with the highest number of fired strips. The highest local occupancy occurs within a jet. If this value is too high, both pattern recognition and impact parameter performance will be degraded, resulting in a loss of b-tagging efficiency and consequent physics reach.

Average occupancy, defined as the number of channels above threshold divided by the total number of channels in a given layer, in MB events with and without noise as a function of radius is shown in Figure 159. The plot clearly demonstrates that the average occupancy due to physics processes in MB events is of about an order of magnitude less than that due to noise in the system. The occupancy caused by hits from real particles drops with radius as expected, and the noise occupancy practically does not change with radius. This behavior is in part due to the relatively low threshold used for the study.

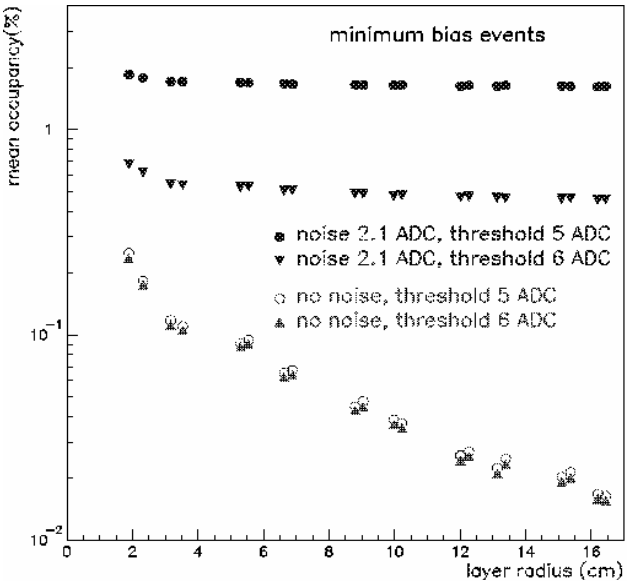


Figure 159 - Mean occupancy as function of radius in minimum bias events without noise and with average noise.

Figure 160 represents the z-dependence of the average occupancy for WH events without noise in the system. It decreases by 50% for layer 0 away from $z=0$. At large z, two silicon modules in layers 2 through 5 are bonded to each other ("ganged") to minimize cable count. Occupancy for these layers clearly increases in the outer barrels where ganging is applied, but not to a level that harms detector performance.

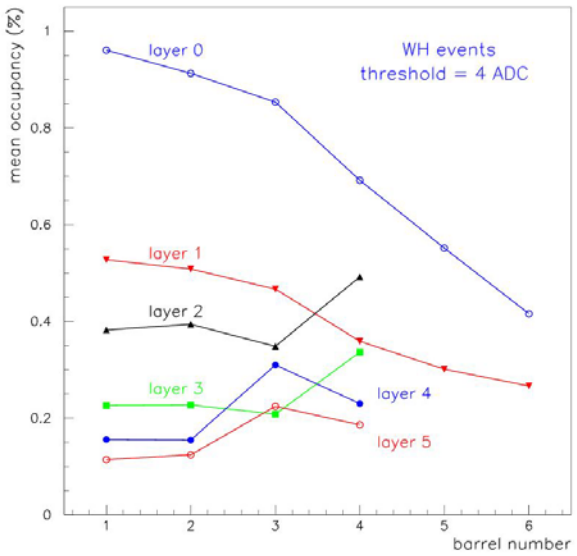


Figure 160 - Mean occupancy as function of z-position of a silicon module at different radii. Higher barrel number corresponds to higher z values.

Dependence of the average occupancy on the readout threshold is shown in Figure 161 for WH events without pile-up. A reduction factor of 1.8 in the average occupancy can be obtained by using a threshold of 5 ADC counts. An additional reduction factor of two can be achieved by using the readout threshold of 6 ADC counts. This does not significantly affect the signal readout efficiency while the S/N ratio is higher than 10:1; but losses of efficiency would be expected for smaller S/N ratios.

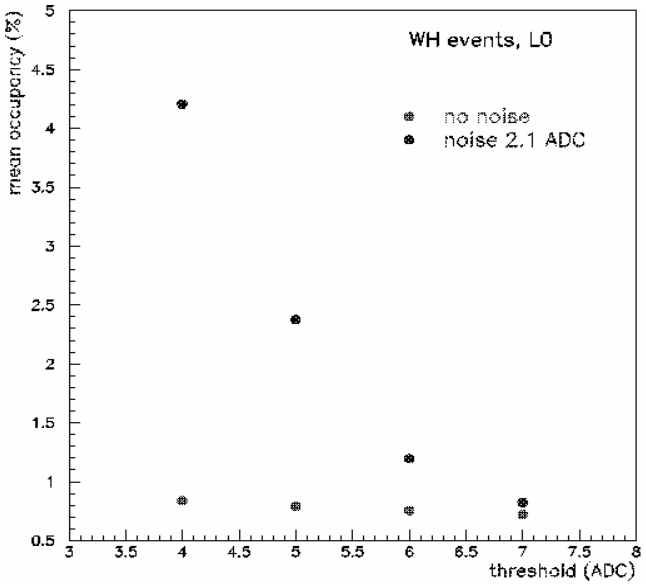


Figure 161 - Mean occupancy in layer 0 without noise and with average noise as a function of the readout threshold.

Peak occupancy as a function of radius for b-jets in WH+0 MB events is shown in Figure 162. At small radii (less than 5 cm), peak occupancy drops from 8% in layer 0 to 6% in layer 1b. For larger radii occupancy is nearly independent of radius since the size of the b-jet is smaller than the area of a module. Dependence of the peak occupancy on luminosity is shown in Figure 163. At higher luminosities, corresponding to the additional 6 MB events, peak occupancy increases by a factor 1.5 in all layers compared to low luminosity case.

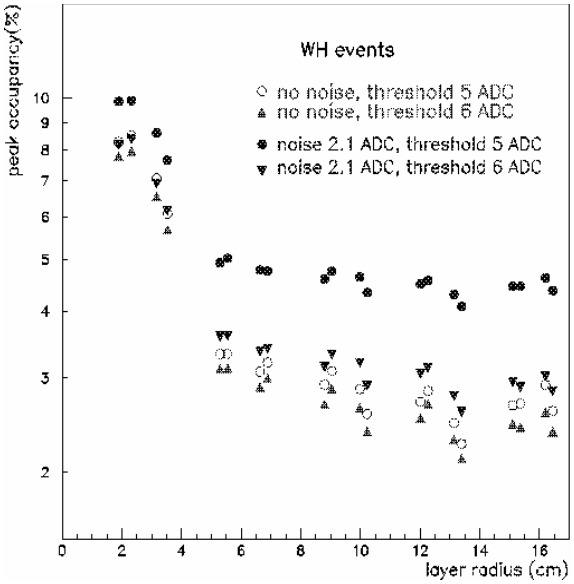


Figure 162 - Peak occupancy without noise and with average noise at different readout thresholds as function of the radius.

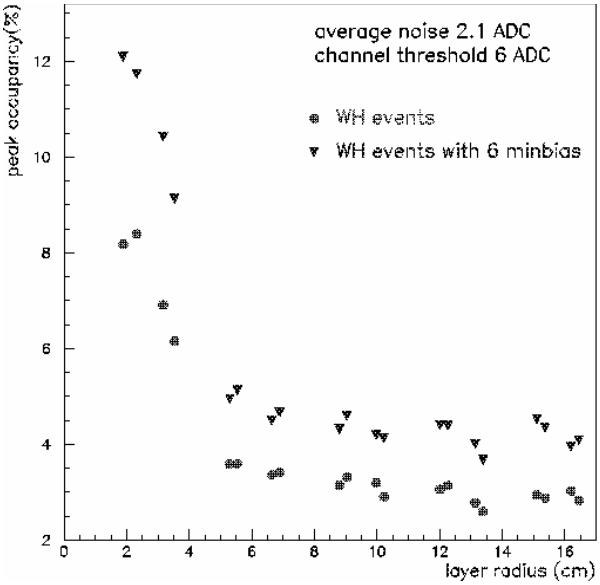


Figure 163 - Peak occupancy in WH events without pile-up and with 6 minimum bias events as function of the radius.

9.6.2 Cluster size and spatial resolution

Spatial resolution plays an important role in the impact parameter resolution and in pattern recognition. Factors determining spatial resolution include detector pitch, presence of intermediate strips, signal-to-noise ratio, the clustering algorithm, Lorentz angle, and direction of the track.

The two inner layers are equipped with 50 μm pitch sensors, and the outer four layers contain sensors with 60 μm pitch. Figure 164 shows the fraction of clusters as a function of number of strips for single muons in the inner and outer layers. Intermediate strips cause two-strip clusters to dominate, leading to an intrinsic single cluster resolution of about 6 μm. Fractions of one-, two- and three-strip clusters are shown in Table 28 together with expected spatial resolutions. Resolutions derived from one- and three-strip clusters are given in Figure 165 and Figure 166, and are approximately the same for inner and outer layers. No mis-alignment of the silicon detectors was assumed.

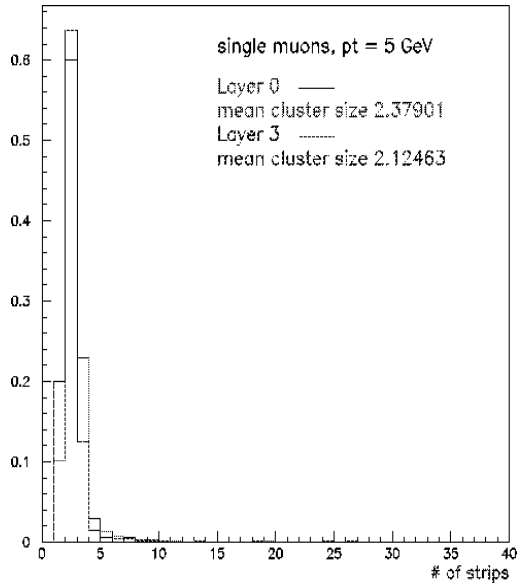


Figure 164 - Cluster size distribution in layer 0 with 50μm readout pitch and layer 3 with 60μm readout pitch.

Table 28 - Position resolutions for various cluster sizes.

	Layers 0,1			Layer 2-5		
Number of strips	1	2	3	1	2	3
Fraction of clusters	0.045	0.49	0.29	0.08	0.52	0.23
Resolution (μm)	12.7	10.9	11.7	12.9	11.1	12.8

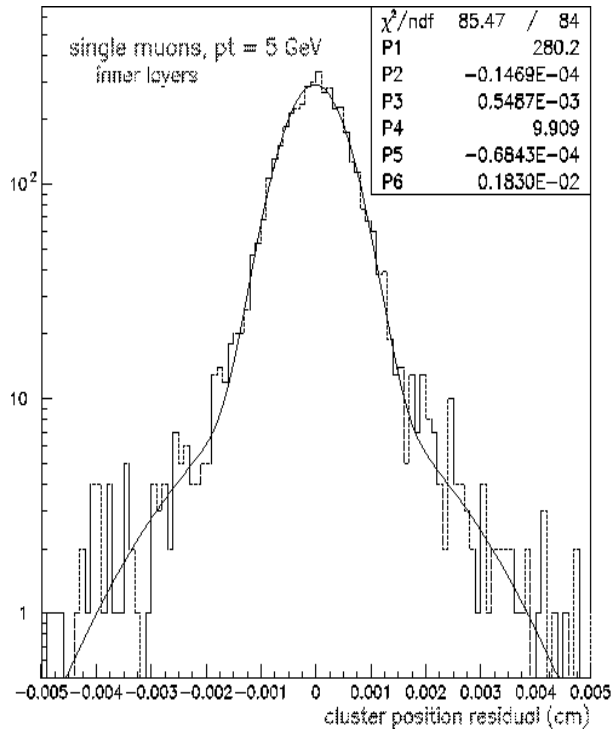


Figure 165 - Spatial resolution derived from the clusters in the two innermost layers with readout pitch of 50 μm.

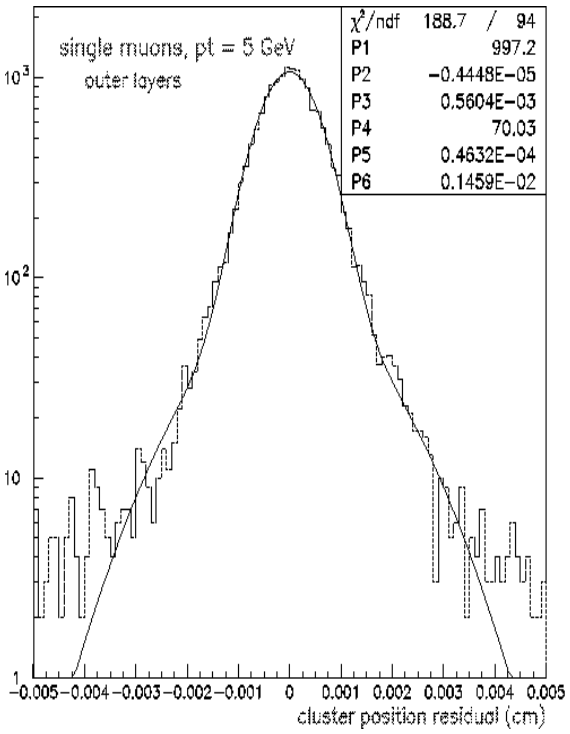


Figure 166 - Spatial resolution derived from the clusters from four outer layers with readout pitch of 60 μm.

Figure 167 and Figure 168 show distributions of the number of strips in clusters for WH and WH events with pile-up. The average number of strips per cluster for physics events is higher than for single muons.

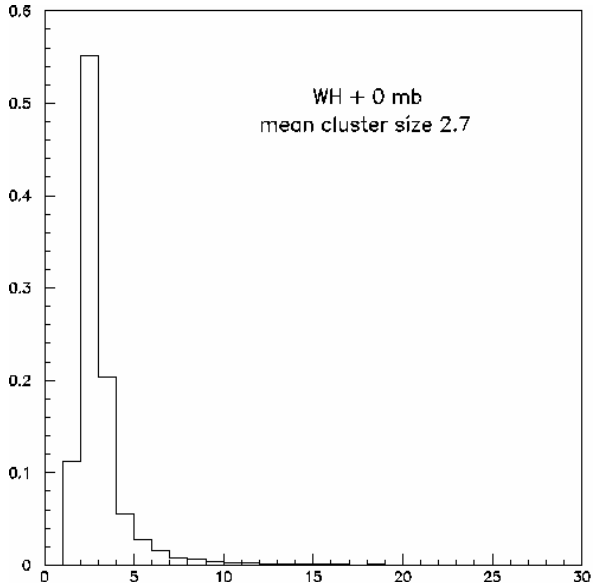


Figure 167 - Cluster size (number of strips) in WH events without pile-up.

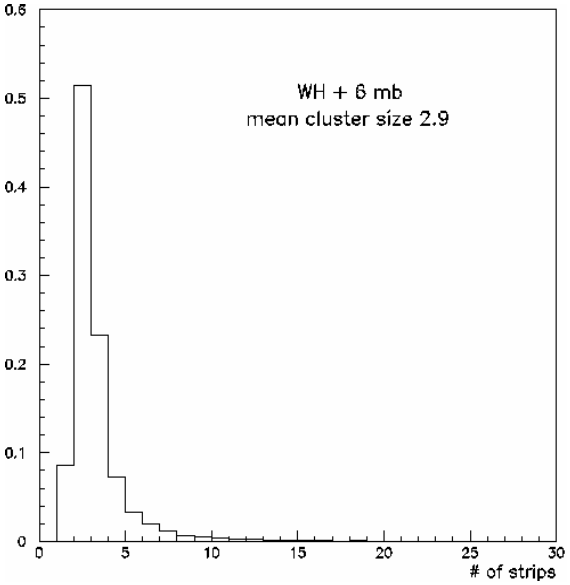


Figure 168 - Cluster size (number of strips) in WH events with an additional 6 minimum bias events.

Clusters formed by more than one track are denoted as "shared clusters". Cluster sharing leads to worse spatial resolution, reduced ability to find tracks close together, and a drop of impact parameter resolution and b-tagging efficiency in the end. The spatial resolution for clusters produced by one track is about 12 μm (Figure 169) while the hit position resolution in the inner layers for WH events for shared clusters is about 27 μm (Figure 170). Figure 171 shows the probability for *N* tracks to share a reconstructed cluster as a function of *N*. This high multi-track correlation effect does not easily reveal itself in simple parametric Monte Carlo studies performed with tools such as MCFast.

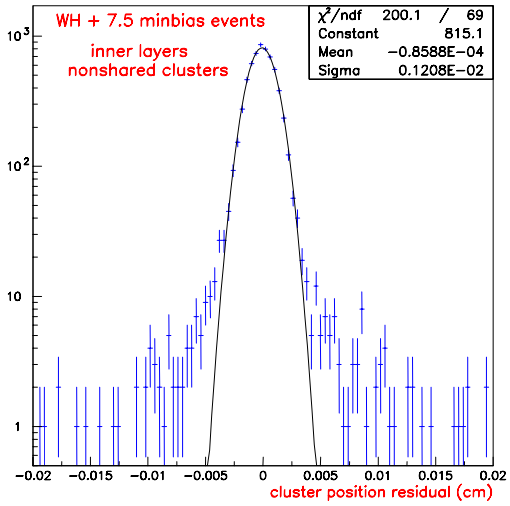


Figure 169 - Hit position resolution in WH events obtained with non-shared clusters.

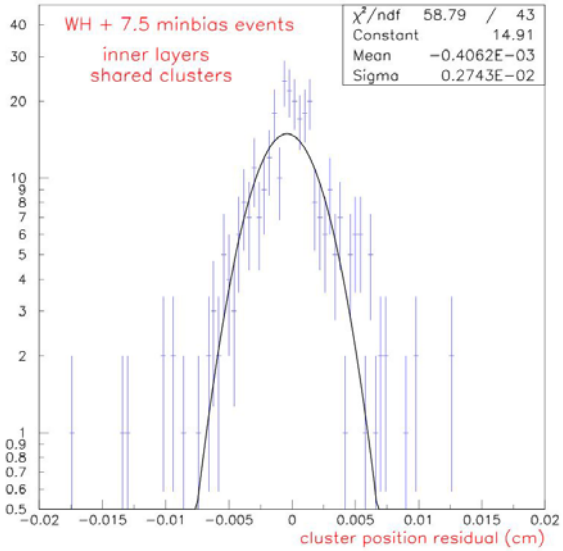


Figure 170 - Hit position resolution in WH events obtained with shared clusters.

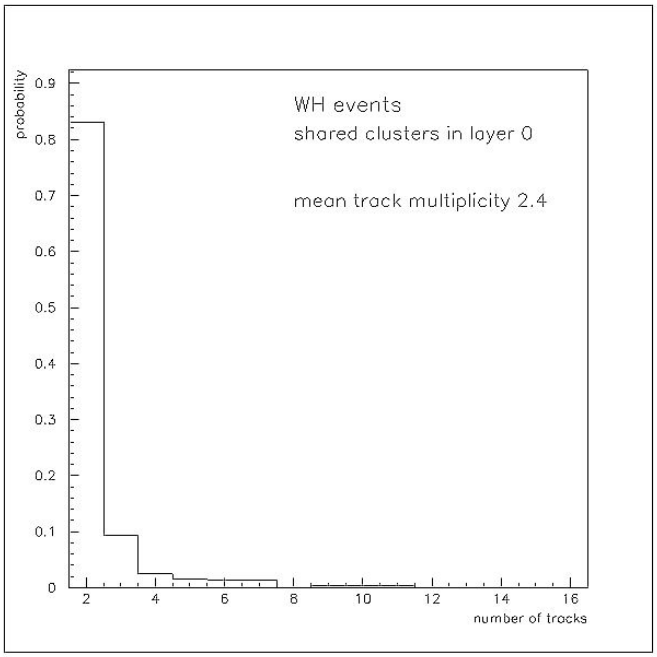


Figure 171 - Average multiplicity of the tracks that form a shared cluster.

The fraction of shared clusters is shown in Table 29 for WH and WH events with pile-up for different layers. The largest cluster sharing of about 6% is observed in layer 0. The fraction of shared clusters decreases with radius for the inner layers and is almost constant for the outer ones since the separation of tracks in b-jets increases modestly over the silicon detector volume.

Table 29 - Percentage of shared clusters vs. layer for WH events with and without 7.5 MB events overlaid.

	L0a	**L0b**	**L1a**	**L1b**	**L2a**	**L2b**	**L3a**	**L3b**	**L4a**	**L4b**	**L5a**	**L5b**
WH events	7.0	4.6	3.8	3.1	2.6	2.2	1.3	1.5	1.3	1.0	1.1	1.0
WH with 7.5 MB	7.5	4.7	3.5	3.0	3.0	2.3	2.0	1.8	1.4	1.2	1.3	1.0

Figure 172, Figure 173, and Figure 174 provide more detail on the spatial resolution of clusters as a function of the number of tracks in the cluster. The resolution degrades rapidly as the number of tracks per cluster increases.

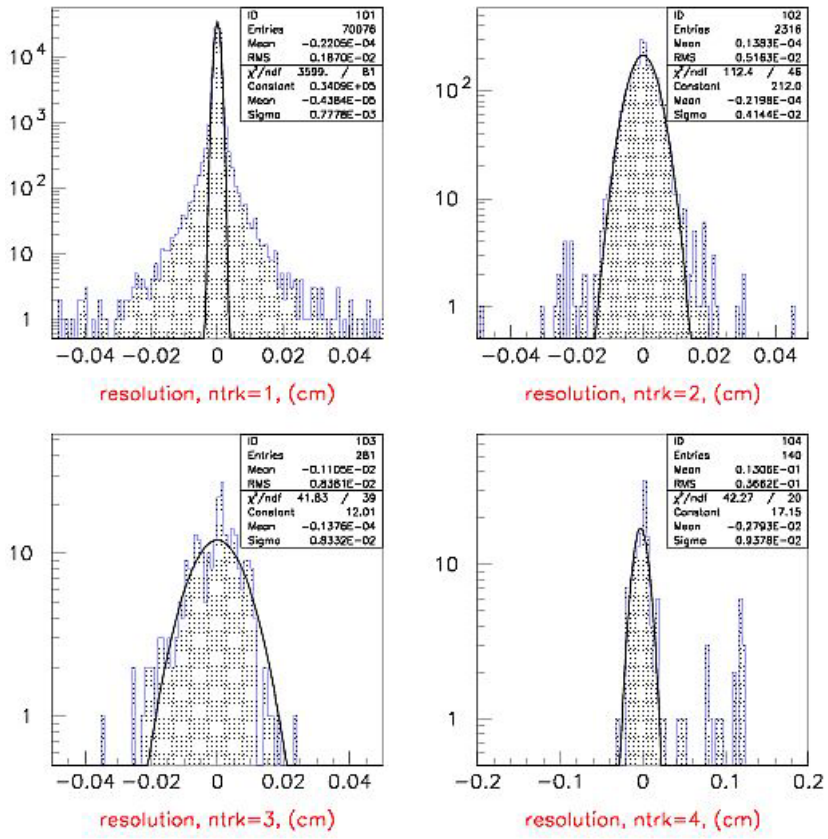


Figure 172 - Distributions of reconstructed-true position for simulated Run IIb SMT clusters for 1, 2, 3, and 4 track clusters.

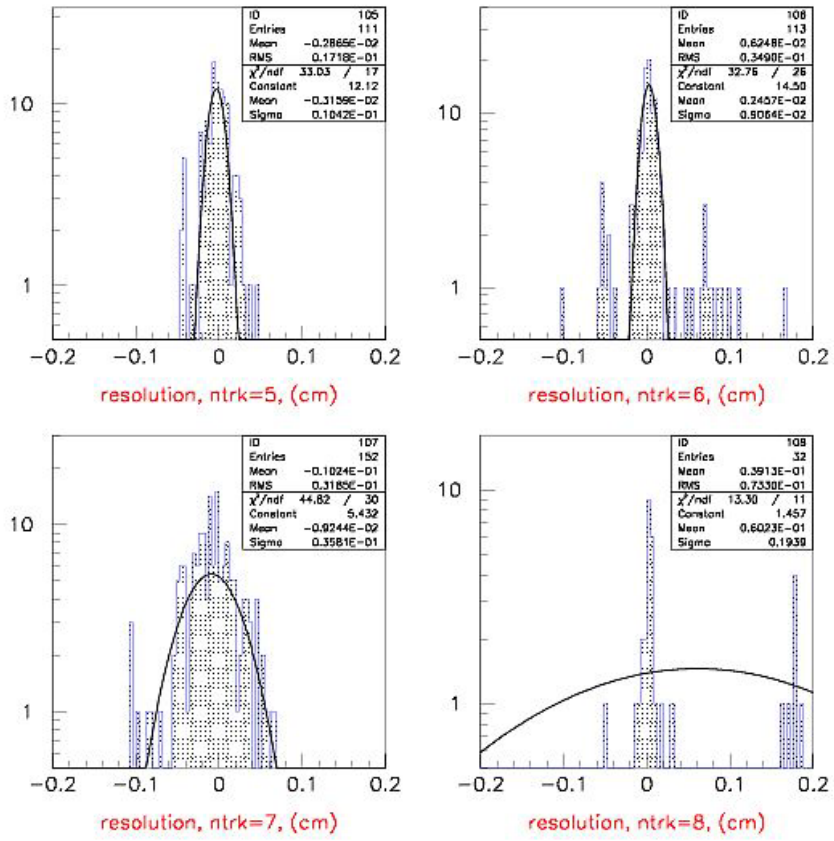


Figure 173 - Distributions of reconstructed-true position for simulated Run IIb SMT clusters for 5, 6, 7, and 8 track clusters.

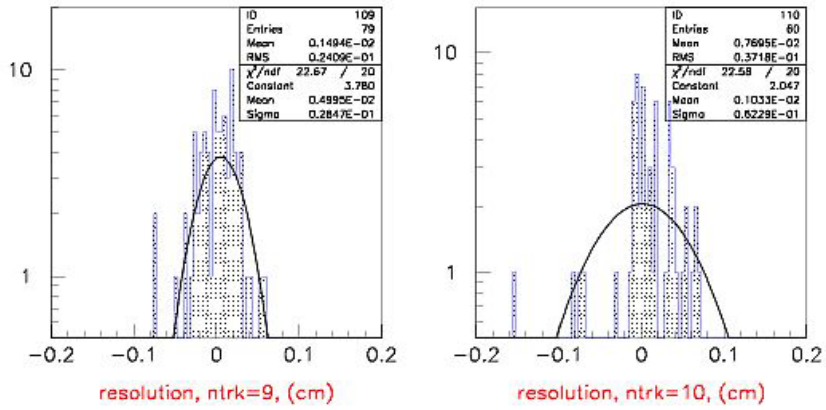


Figure 174- Distributions of reconstructed-true position for simulated Run IIb SMT clusters for 9 and 10 track clusters

9.7 Physics Performance of the Run IIb Tracker

As discussed earlier in this document, the main Run IIb physics goal is the search for the Higgs boson. Other important investigations will center on top-quark properties, precision measurements of W-boson mass and width, b-physics, and searches for supersymmetry and other new phenomena. All physics would benefit from improved track reconstruction efficiency and momentum resolution in a Run IIb tracker with an upgraded silicon detector. However, higher b-tagging efficiency keys new physics discovery potential in DØ.

It is worth summarizing the essentials of simple cuts-based search for WH. Requirements include:

1. A high p_T lepton of at least 20 GeV with $|\eta|<2$ and a missing $E_T>20$ GeV. This strongly suppresses all final states without a W or Z, selecting ttX, WX, and ZX.

2. No other isolated tracks with $p_T>10$ GeV. This suppresses events with $Z\rightarrow ll$ and $tt\rightarrow llX$.

3. No more than two central jets with $E_T>20$ GeV. This suppresses $tt\rightarrow bl\nu bjj$.

4. At least two tagged b-jets. This suppresses $Wjj\rightarrow l\nu jj$ and $WZ\rightarrow l\nu jj$

Note that the suppression of QCD events is largely accomplished without b-tagging in this final state. The largest backgrounds turn out to be contributions from $Wbb\rightarrow l\nu bb$, $WZ\rightarrow l\nu bb$, and $tt,tb\rightarrow l\nu bb(nj_{miss})$ that cannot be reduced by any improvement in the SMT. The irreducibility of the backgrounds (at least without a more sophisticated analysis) implies that S/B will be independent of the b-tagging efficiency and that S/sqrt(B) will be linear(not quadratic) in single b-jet tagging efficiency.

The following sections summarize the track reconstruction efficiency, accuracy of the track parameter measurements, and b-tagging efficiency obtained from studies of WH events.

9.7.1 Single track performance

The p_T resolution $\sigma(p_T)$ for single muons is shown in Figure 175, together with $\sigma(p_T)$ calculated for the Run IIa tracker. Resolution is obtained from a Gaussian fit to q/p_T, where q is the particle charge. No tails were observed in this distribution for single muons. For low p_T, where the p_T resolution is dominated by multiple scattering there is no difference between Run IIa and Run IIb trackers. An improvement at high p_T is observed due to larger number of precise measurements per track. The difference is big at small $|\eta|$ and disappears at $|\eta|$ above 1.5, as it is shown in Figure 175 (left).

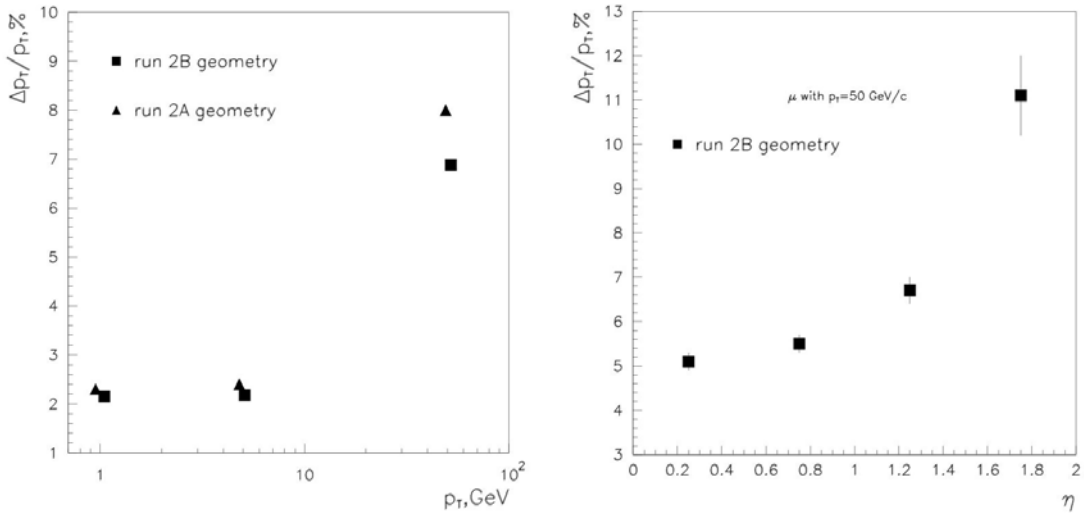


Figure 175 - p_T-resolution as a function of p_T (left) and function of pseudorapidity (right) for single muons in Run IIa and Run IIb.

Reconstruction efficiency as function of |η| is shown in Figure 176. It is fairly flat up to |η|=1.5 for all transverse momenta. Because tracks at larger η miss the fiber tracker altogether and cannot produce the minimum four hits required for silicon-only tracking, the reconstruction efficiency begins dropping above |η|=1.5, falling to 90% by |η|=2.

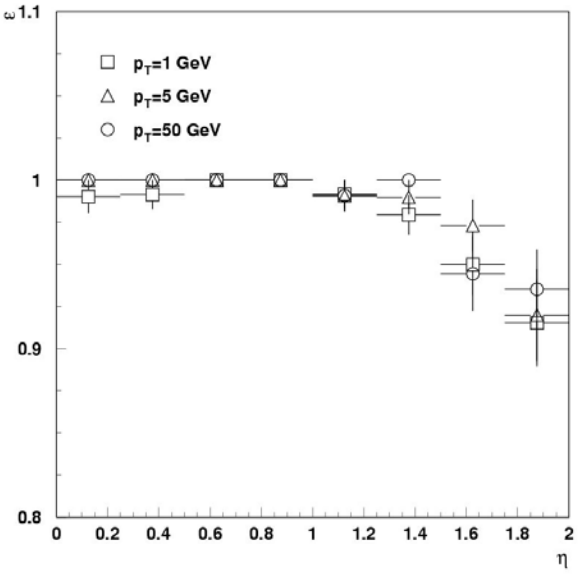


Figure 176 - Reconstruction efficiency as function of η of muons with pT=1,5,and 50 GeV/c.

Impact parameter resolutions in the transverse plane and *z*-direction are important for heavy-flavor tagging, primary vertex reconstruction (especially at high luminosity), and detection of secondary vertices. At high momenta (p_T>10 GeV), resolution is determined to a large extent by the measurements in layer 0. At smaller momenta, it depends on multiple scattering and therefore the material distribution in the tracker. Transverse impact parameter resolution as function of p_T of single muons is compared to that in Run IIa in Figure 177. Improvement by a

factor of 1.5 is expected for $\sigma(d_0)$ over the whole p_T region. This can be understood as being due to the closer (to the interaction point) first measurement in the Run IIb silicon detector and to the larger number of precision measurements. Indeed, for a simple two layer detector with measurements of hit resolution σ_{meas} at radii R_{inner} and R_{outer}, the impact parameter resolution is simply $\sigma(d_0) \sim \sigma_{meas}(1+R_{inner}/R_{outer})$. The ratio R_{inner}/R_{outer} is 0.27 in Run IIa and 0.11 in Run IIb. This geometric change accounts for almost all of the impact parameter resolution improvement.

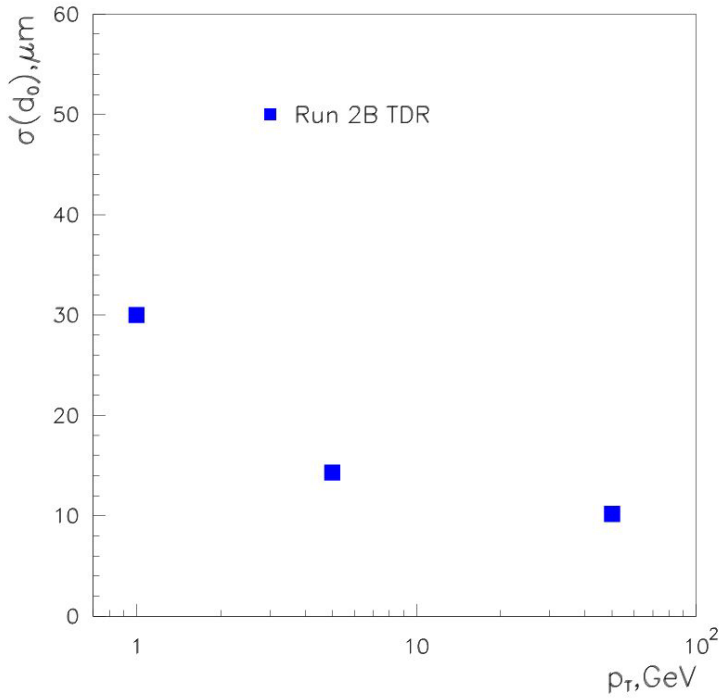


Figure 177 - Transverse impact parameter resolution as function of pT for single muons.

The transverse impact parameter resolution $\sigma(d_0)$ as function of $|\eta|$ is shown in Figure 178 for the Run IIb tracker. For Run IIb, a slight degradation in $\sigma(d_0)$ is observed for low-p_T tracks with increasing $|\eta|$; for high-p_T tracks the distribution of transverse parameter resolution vs. $|\eta|$ is flat. These behaviors are expected from the enhanced contribution of multiple scattering at large $|\eta|$ and small p_T

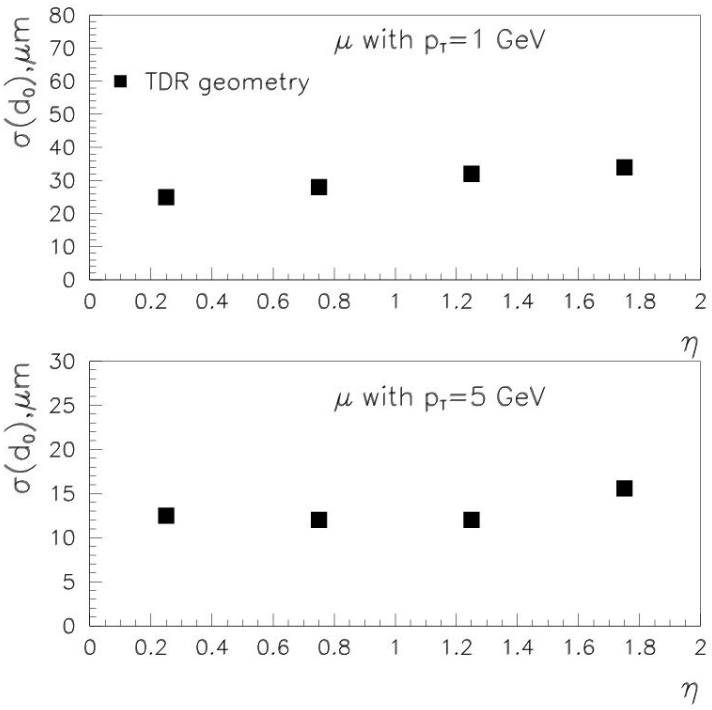


Figure 178 - Transverse impact parameter resolutions in Run IIb for low-pT muons.

Dependence of the longitudinal impact parameter resolution on p_T is shown in Figure 179. Because of the absence of three-dimensional measurements in layer 0 and the relatively worsened *z*-resolution obtained with 2° stereo detectors compared to the 90° detectors in Run IIa, the resolution in longitudinal impact parameter resolution in Run IIa degrades to 280 μm for high-p_t muons.

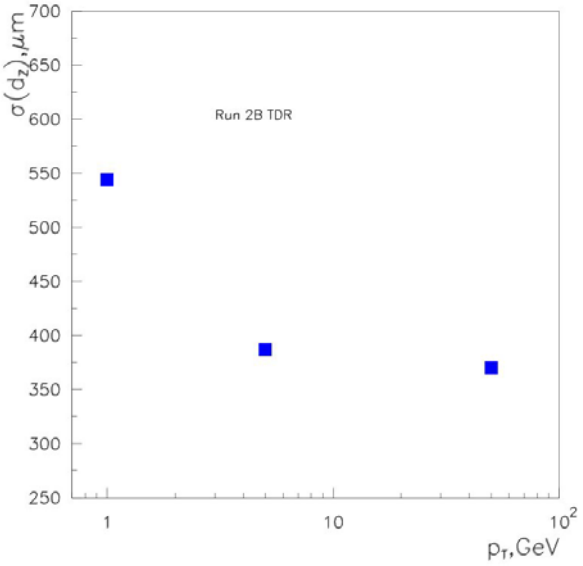


Figure 179 - Longitudinal impact parameter resolution as a function of pT for single muons.

9.7.2 b-tagging performance

B-tagging is the main tool for searches for the Higgs boson and many supersymmetric objects, as well as for top physics. The main goal of b-tagging methods is to reject jets produced by light quarks and gluon jets while preserving a high efficiency for tagging of the b-jets. Pre-selection of b-jets is based on the relatively long lifetime of B hadrons. Rejection of charm jets is limited by the finite lifetime of charmed hadrons, and rejection of gluon jets is bounded by contributions from gluon splitting to heavy quarks at branching fractions of a few percent. Experimental limitations for ideal b-tagging arise from inefficiencies of the track reconstruction in jets, impact parameter resolution and secondary vertex resolution.

The overall track reconstruction efficiency in jets together with the corresponding fake track rate is presented in Table 30 for WH events at low and high luminosities. There is slight degradation in the track finding efficiency at high luminosity, but the fake track rate is negligible in both cases. The average track reconstruction efficiency in jets $\varepsilon_{tr\text{-}j}$ is consistent with that for Run IIa.

Table 30 - Track reconstruction efficiency $\varepsilon_{tr\text{-}j}$ and fake track rate in jets in WH events without pile-up and with 7.5 MB events.

	$\varepsilon_{tr\text{-}j}$	***Fake rate***
WH + 0 min bias events	83%	<0.01%
WH + 7.5 min bias events	81%	0.1%

Figure 180 shows $\varepsilon_{tr\text{-}j}$ as function of the jet $|\eta|$ for WH+0MB and WH+6MB events. The behavior of $\varepsilon_{tr\text{-}j}$ in jets is similar to the single-track performance. It is high (~88%) in the central region and quickly degrades beyond the fiber tracker boundary to ~60% at $|\eta|$=2. The relative drop in efficiency for higher $|\eta|$ is more pronounced in jets than observed for isolated muons. That can be explained by the fact that the more energetic jets at higher $|\eta|$ produce higher track multiplicity, making pattern recognition more complicated. Taking into account that b-quarks from Higgs boson decays and top decays produce mostly central jets, one can expect the overall performance to be dominated by a track reconstruction efficiency in jets of 85-88%.

A signed impact parameter (SIPtag) method[40] was used to evaluate b-tagging performance. A SIPtag requires that:

- Tracks lie within a cone $\Delta R < 0.5$ around the jet axis;
- Selected tracks have $p_T > 0.5$ GeV/*c*, good reconstruction quality, and at least two hits in the silicon;

[40] A. Khanov, R. Demina "Histogramming Track Finder: The impact parameter b-tagging performance", DØ Note 3855.

- At least two tracks have an impact parameter significance $S= d_0/\sigma(d_0)>3$ or at least three tracks have S>2.

To estimate the "true" b-tagging efficiency the numbers of b, c, and s and u-d quarks with E>20 GeV and $|\eta| <2$ were counted; and their parameters were compared to those of tagged b-jets. If a tagged jet was within a cone distance $\Delta R<0.5$ about one of the light quarks, the flavor of that quark was assigned to the jet.

The b-tagging efficiency ε_b is defined as the ratio of the number of jets with assigned b-flavor to the total number of b-quarks in the considered acceptance. The mis-tagging rate is defined as the ratio of the number of b-tagged jets originating from light quarks to the total number of jets produced by light quarks in the considered $(E,\eta)_{jet}$ acceptance.

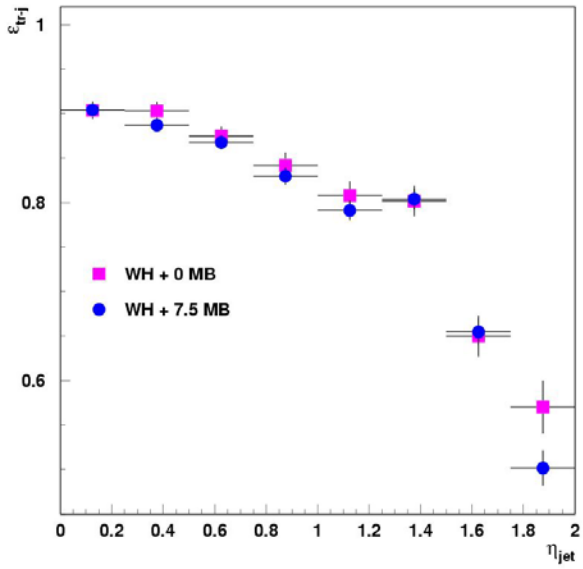


Figure 180 - Track reconstruction efficiency in b-jets as function of jet $|\eta|$.

Figure 181 shows the b-tagging efficiency ε_b vs. $|\eta|$ of the reconstructed b-jets in WH +0 MB events. The average ε_b per jet of 69% is 19% higher than in Run IIa. This is a consequence of the improved impact parameter resolution due to the presence of layer 0. The b-tagging efficiency is above 70% for $|\eta|<1$, reflecting the high track reconstruction efficiency in jets in that region. It decreases with increasing $|\eta|$ to 45% at $|\eta|=2$. Dependence of the mis-tagging rate on the jet $|\eta|$ was studied using Z-boson decays to first generation quarks; it is shown in Figure 182. The mis-tagging rate varies between 1% and 2% over the whole $|\eta|$ region. No $|\eta|$-dependence of mis-tagging rate in Run IIb is observed within errors.

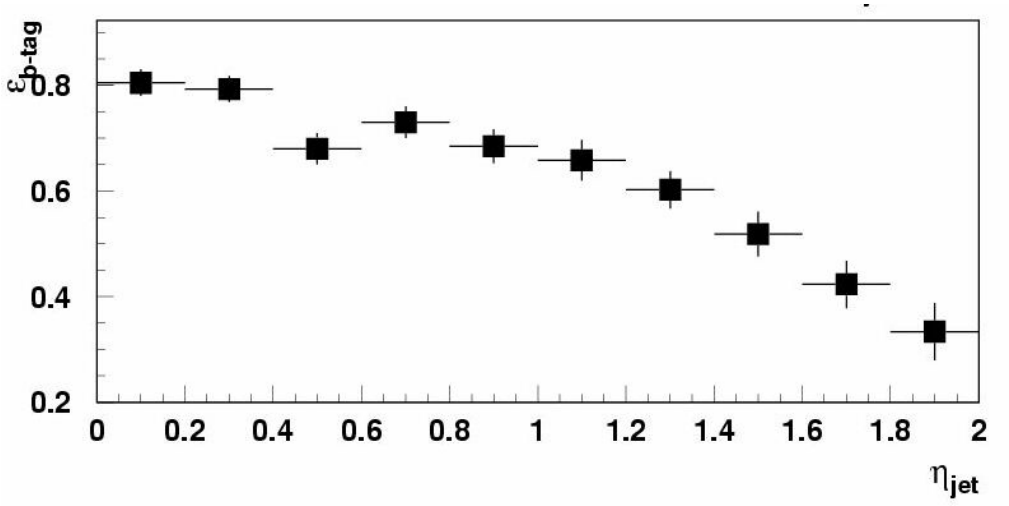


Figure 181 - b-tagging efficiency as function of $|\eta|$ of the tagged jet.

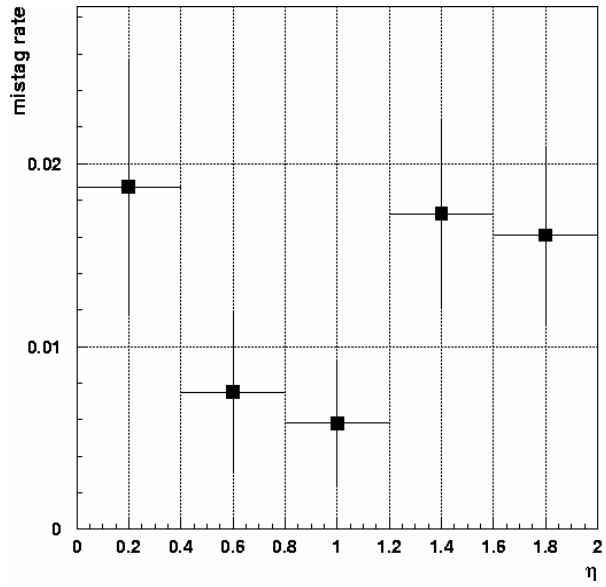


Figure 182 - Mis-tagging rate as function of $|\eta|$ of the tagged jet.

Dependencies of the b-tagging efficiency and the mis-tagging rate on reconstructed jet energy E_j are shown in Figure 183 and Figure 184, respectively. The best performance in terms of b-tagging is expected for jets with $E_j \sim 70$-100 GeV. The rise of efficiency above 150 GeV is not statistically significant. Due to insufficient statistics, the mistagging rate is estimated only up to 140 GeV and is demonstrated to be about 1.5 % in the whole considered energy scale.

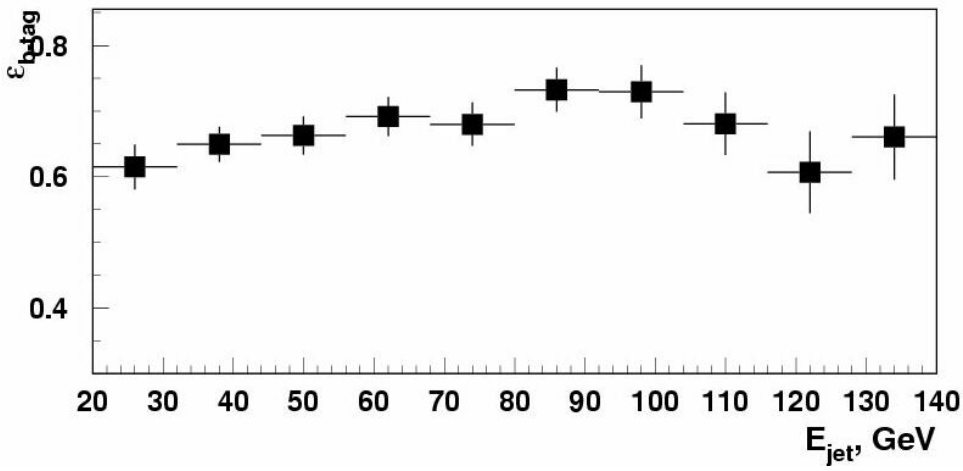


Figure 183 - b-tagging efficiency as function of the energy of the tagged jet.

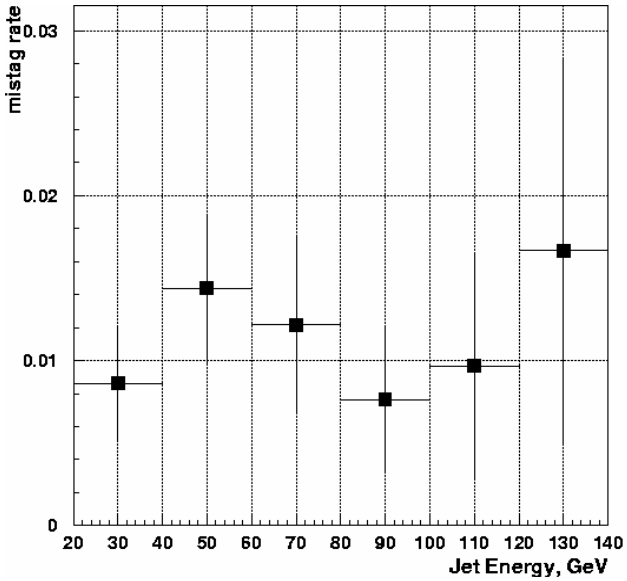


Figure 184 - Mis-tagging rate as function of the energy of the tagged jet.

Probabilities to tag an event with one or two b-jets are shown for Run IIa (estimated from Z-boson decays to bb) and Run IIb (from WH events) in Table 31.

Table 31 - Probabilities to tag an event with one or two b-jets.

	Run IIa	***Run IIb***
$P(n_b \geq 1)$	68%	76%
$P(n_b \geq 2)$	21%	33%

One can see from the table that an essential improvement in the selection of events with b-tagged jets can be achieved with the Run IIb tracker as compared to the existing tracker. Taking into

account the lower mis-tagging rate obtained in the Run IIb geometry, one can conclude that the signal-to-background ratio in all analyses involving b-jets will be significantly better in the next run.

Because of the slight degradation of track reconstruction efficiency in jets with increasing luminosity, the b-tagging efficiency per jet (ε_b) deteriorates from 69% without pileup to 66% with an additional six MB events. This leads to the slightly decreased values $P(n_b \geq 1)$=76% and $P(n_b \geq 2)$=33%. Mis-tagging rates were not seen to increase significantly at higher luminosity.

9.8 Conclusions

The Run IIb silicon detector demonstrates good physics performance in a realistic simulation that includes detailed physics and detector response modeling and full pattern recognition. The physics performance studies prove that the proposed silicon design meets the requirements of the physics program of DØ Run IIb.

Detailed studies of occupancy in the Run IIb silicon detector show the expected higher rates (about 12% for busy events) in the inner layers. However, no accompanying worsening in the spatial resolution of hits is seen. Only 6% of reconstructed clusters in layer 0 are expected to be shared by more than one track. The remaining single hit clusters determine a single hit position with an accuracy of 12 μm.

The choice of small-degree stereo detectors leads to a significant decrease in ghost tracks and a consequent improvement in pattern recognition. The additional layer 5 at radius R=16.4 cm helps to improve p_T resolution for non-central tracks. The new layer 0 at a small radius results in a factor of 1.5 improvement in impact parameter resolution. As a consequence the single b-tagging efficiency per jet improves by 19% compared to that obtained with Run IIa; and the percentage of events with two b-tagged jets will be 67% higher than in Run IIa at a fixed mis-tagging rate.

Predictions made for discovery limits of the Higgs boson in Run IIb were based on the assumption that DØ would have the same performance as in Run IIa. The proposed silicon detector is shown to deliver even better performance for high-p_T processes.

10 SUMMARY

A design effort within DØ has been proceeding for the past two years to build a new silicon detector capable of exploiting the physics potential available with the Tevatron Run IIb. The design studies for this new silicon detector were carried out within a set of stringent boundary conditions set by the Laboratory and the high-energy physics program world-wide. The design has also been guided by the desire to retain as much as possible of the existing data acquisition system. Even though these constraints are significant, the new detector presented in this document is designed to have better performance than the Run IIa detector and can be built expeditiously.

The proposed silicon detector has a 6 layer geometry arranged in a barrel design. The detector will be built in two independent half-modules split at z=0. The six layers, numbered 0 through 5, are divided in two radial groups. The inner two layers (layers 0 and 1) will have axial readout only. The sensors for these layers will be mounted on carbon fiber support structures with integrated cooling. Due to the stringent cooling requirements for layer 0, the readout hybrids will not be mounted on the silicon sensors, as is the case for all other layers, but be mounted outside of the tracking volume on a separate hybrid support structure. Fine pitch, lightweight, flexible analog cables will be used to carry the layer 0 signals out of the tracking volume. The basic element of the outer layers, layers 2-5, is a 'stave'. A stave consists of a core which carries the cooling lines, with sensors mounted on both sides of the stave core. One side of the stave will have axial readout, and the other side stereo readout. The stereo angle is obtained by rotating the sensors. Each stave carries six sensors on each side.

The electrical signals from the silicon sensors are presented to hybrids, which carry the readout chip. The SVX4 chip will be used to acquire, digitize and readout the silicon signals. Except for layer 0, all hybrids are double-ended. That is, each hybrid will collect the signals from two independent readout segments. This design choice was motivated by the desire to minimize the cable plant, since the existing cable plant will be re-used for the new detector. Digital jumper cables carry the signals from the hybrid to a Junction Card. At this junction the signals are transferred to a twisted pair cable which carries the signals to an Adapter Card. The Adapter Card is the place where the new data acquisition system will interface with the existing data acquisition and cable plant. First versions of all elements of the readout chain have been obtained, as described in this report, and to date no major issues were uncovered in their testing.

The proposed silicon detector will use only single-sided silicon. There are a total of 2304 silicon sensors in this design, read-out with 888 hybrids containing 7440 SVX4 chips. For comparison, the Run IIa silicon detector has 793K readout channels while the Run IIb one will have 952K readout channels. The Run IIb silicon detector is designed to allow faster construction due to fewer and simpler parts than the Run IIa device. For example, all staves in our design are identical and there are only three types of sensors foreseen for the whole detector.

The physics performance studies prove that the proposed detector design meets the requirements of the physics program of DØ Run IIb. The choice of small-degree stereo detectors leads to a significant decrease in ghost tracks and thus improved pattern recognition. Compared to the Run IIa detector, the new detector has an improved utilization of the outer radial region and has added a layer at a very small radius. Layer 5 at a radius of 16 cm helps to improve the p_T resolution for

non-central tracks. Layer 0 at a radius of about 18 mm results in a factor of 1.5 improvement in impact parameter resolution. As a consequence, the single b-tagging efficiency per jet improves by 19% compared to that obtained with Run IIa, and the percentage of events with two b-tagged jets at fixed mistag rate will be 14% higher than in Run IIa. With the new detector we will also have better stand-alone silicon tracking. Predictions made for discovery limits of the Higgs boson in Run IIb were based on the assumption that DØ would have the same performance as in Run IIa. The proposed detector is shown to be well-matched to the search for the Higgs boson and the study of a wide variety of high-p_T processes.

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